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Research Paper

Adaptive Phase-Locked Loop Utilizing Sliding Discrete Fourier Transform for Accurate Synchronization and Enhanced Power Quality within Distribution Networks

Alireza Rostamipour * and *Mehdi Abdi*

Department of Electrical Power Engineering, Islamic Azad University Mashhad Branch, Mashhad.

Abstract— *This study presents an advanced Frequency Adaptive Sliding Discrete Fourier Transform-based Phase-Locked Loop (FASDFT-PLL) for grid synchronization and power quality enhancement in distribution networks. Traditional PLL techniques, such as SDFT-PLL and MSTOGI-PLL, often struggle with phase inaccuracies, slow convergence, and poor tracking under distorted grid conditions or frequency variations. The proposed FASDFT-PLL dynamically adjusts the observation window size in real time, enabling accurate extraction of the fundamental voltage component, phase angle, and frequency, even with various zero crossings, harmonics, and nonlinear loads. To validate its performance, the method is tested under multiple conditions. Compared to conventional techniques, FASDFT-PLL exhibits faster convergence, higher phase tracking accuracy, and improved robustness against frequency deviations and harmonic distortions. The proposed method is further integrated with a shunt active power filter (SAPF), demonstrating its effectiveness in maintaining power quality and reducing harmonic distortion. Simulation results confirm that FASDFT-PLL significantly outperforms existing PLL algorithms, making it a promising solution for modern power systems.*

Keywords—FASDFT, phase-locked loop, active filters, power quality, harmonic reduction.

1. INTRODUCTION

The rapid advance of technology has led to a dramatic increase in the use of diverse power electronic devices, including switch mode power supplies for efficient energy conversion, adjustable speed drives for precise motor control, programmable logic controllers for automated processes, refrigerators for smarter food storage, inverters for renewable energy integration, and energy-efficient lighting systems for eco-friendly illumination. However convenient they may be in their functionality; it cannot be overlooked that such entities possess non-linear features which exert a detrimental impact on the quality of power within distribution systems. An inherent distortion is introduced into both voltage and current waveforms as a direct consequence of their operation. While volumes in literature delineate numerous proposed remedies to address this predicament, the shunt active power filter (SAPF) stands as an unrivaled method extensively embraced for its capacity to substantially improve this situation [1, 2]. To tackle these quandaries, scholars have put forth a novel advancement known as the transformer-integrated filtering system. This groundbreaking development boasts various benefits, including decreased loss of power in transformers, superior capacity for eliminating harmonics, and reduced spatial requirements. Nevertheless, the tainted grid presents a fresh hurdle when it comes to maintaining power quality. The age-old approach of extracting unit templates or phase angles directly from distorted voltage signals proves ineffective due to the presence of imbalanced and distorted grid voltage influenced by harmonics and noise. Therefore, it becomes imperative to delve into enhanced and efficacious techniques for detecting the fundamental components of voltage, frequency, and phase angle [3].

A synchronization technique ought to possess the capability to promptly react to alterations in the electrical grid, reliably assess the phase angle of the said grid, proficiently discern any variations in its frequency, and skillfully isolate harmonic elements as well as disruptions from the fundamental waveform.

Within the realm of synchronization techniques, two prominent categories emerge: those that hinge upon phase-locked loop (PLL) methodology, and those divergent from such principles. The literature review delves into a comprehensive analysis of various PLLs employed in three-phase as well as single-phase systems. It is worth highlighting the Synchronous Reference Frame-based PLL, the Enhanced PLL, and the Second-Order Generalized Integrator PLL. These influential mechanisms bear immense significance when it comes to harmonizing and facilitating the seamless functioning of grid-connected systems in a meticulously regulated amalgamation [1]. Nevertheless, the precise detection of frequency and phase angle poses a formidable challenge, one that has significant implications for the dependability, functionality, and power integrity of grid-connected systems. Numerous alterations and advancements have been postulated to augment the fundamental three-phase Phase-Locked Loop (PLL), relying upon the tenets of Synchronous Reference Frame-based theory (SRF or d-q theory). While the SRF-PLL excels in maintaining stability during stationary conditions, it falters when confronted with fluctuations in phase, alterations in frequency, or disturbances in waveform. To address this quandary, certain scholars have sought remedies by

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*Corresponding author:
E-mail: alireza.rostamipour@srbiau.ac.ir (A. Rostamipour)
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integrating refined filter designs such as notch filters or moving average filters [4].

However, challenges arise when the inverter must extract phase and frequency data from a grid voltage that is weak and distorted. To address this issue, the Synchronous Reference Frame (SRF) PLL is employed [5]. This well-established concept enables the inverter to accurately track both the phase angle and frequency of the grid voltage, facilitating the generation of a reference signal for power converter control. The main idea of phase locking is to generate a signal that adjusts its phase angle to match variations in the phase angle of a given signal [6]. However, its efficacy diminishes significantly under unbalanced and distorted grid conditions, raising concerns about its stability and operational reliability [7]. Notably, various advanced configurations of PLLs have emerged to mitigate the challenges faced by traditional SRF-PLLs. These include the Decoupled Double Synchronous Reference Frame PLL (DDSRF-PLL) and the Fixed-Reference-Frame PLL (FRF-PLL), which enhance dynamic response and disturbance rejection capabilities in adverse grid environments [8]. The evolution of these advanced PLL designs aims to overcome limitations associated with the traditional SRF-PLL, which can struggle with phase angle detection and synchronization accuracy during asymmetric grid faults, leading to phenomena such as loss of synchronization (LOS) [7, 9].

The SDFT PLL is a cutting-edge solution designed to address the inherent limitations of traditional Synchronous Reference Frame Phase-Locked Loops (SRF-PLLs) used in grid synchronization. The SDFT PLL introduces innovative hybrid filtering techniques, which enhance its resilience and accuracy in these challenging environments, marking a significant advancement in phase-locked loop technology [5, 10]. The advancements in the SDFT PLL have positioned it as a vital tool in modern power electronic systems, particularly in renewable energy applications where grid conditions can be unpredictable. Research has demonstrated the SDFT PLL's superior dynamic performance, achieving convergence times of less than one grid cycle during rapid frequency changes, a feat that conventional PLLs often fail to match [10]. Furthermore, the SDFT PLL effectively manages unbalanced voltages, mitigating common issues associated with traditional PLL designs and ensuring robust synchronization even in less-than-ideal grid scenarios [9].

Several studies have proposed advanced PLL techniques for grid synchronization. In [11], a Multi-Stage Second-Order Generalized Integrator PLL (MSTOGI-PLL) was developed to enhance harmonic rejection. In [12], the SDFT method has shown significant computational efficiency, requiring only one complex multiplication and two additions per time step. This efficiency makes the SDFT particularly suitable for real-time applications where frequency analysis must be performed quickly and with minimal processing resources. In addition, in [13], Improved PLL design methods based on SDFT techniques have been proposed to enhance phase estimation during grid voltage harmonics, reducing steady-state errors in frequency tracking, the findings also extend to applications in grid synchronization and renewable energy sources (RES). Despite the benefits of these advanced PLLs, challenges persist, particularly in the context of off-nominal frequencies. The MSTOGI-PLL suffers from slow response time under sudden frequency variations, making it unsuitable for fast-changing grid conditions. SDFT-PLL assumes a fixed-frequency window, limiting its adaptability when the grid frequency fluctuates beyond a predefined range. Moreover, The SDFT can suffer from spectral leakage, leading to inaccuracies in magnitude and phase angle estimations. This issue is pronounced when the algorithm operates away from its nominal frequency, reducing its harmonic rejection capabilities [14]. Additionally, many traditional PLL methods are highly sensitive to multiple zero-crossing distortions, leading to erroneous phase tracking under high harmonic content.

The proposed FASDFT-PLL addresses these limitations by dynamically adjusting its observation window in real time, allowing it to accurately track phase and frequency variations under severe grid disturbances. Unlike previous methods, it does not rely on fixed-frequency assumptions and can effectively reject harmonics while maintaining fast convergence. This paper presents a thorough analysis of the investigation findings and a comparison with traditional synchronization techniques. The main aims of this study are as follows:

1) Develop a Frequency Adaptive Sliding Discrete Fourier Transform (FASDFT) that accurately extracts voltage fundamental components from the point of common coupling (PCC) voltage, even when faced with fluctuating conditions.
2) To employ the developed Phase-Locked Loop (PLL) in generating unit templates and achieving synchronization in both perfect and distorted grid scenarios.
3) To conduct three tests comparing the effectiveness of the proposed PLL against new recent proposed techniques (SDFT and MSTOGI) when dealing with voltage sag/swell, frequency fluctuations, and changes in phase angle.

The paper is organized as follows: in Section 2, an overview of a shunt active filter connected to a three-phase distribution system aimed at improving power quality is provided. In Section 3, the FASDFT-PLL mathematical formulation is presented. Section 4 focuses on the utilization of the proposed FASDFT-PLL to generate pulses for the Voltage Source Inverter (VSI), which is controlled as a SAPF. In Section 5, simulation results are presented and discussed, highlighting the application of FASDFT-PLL. Finally, Section 6 summarizes the research work's conclusion.

2. System Overview

Fig. 1 illustrates the three-phase distribution system that is utilized for implementing and evaluating the performance of the proposed phase-locked loop (PLL). A three-phase programmable supply creates diverse voltage waveforms, testing FASDFT-PLL performance for load compensation under open-loop and closed-loop conditions. In closed-loop, VSI control is grid-synchronized via the proposed PLL, while a nonlinear load is linked at the PCC, and the SAPF joins through interfacing inductors. Hall-effect sensors monitor voltage and current.

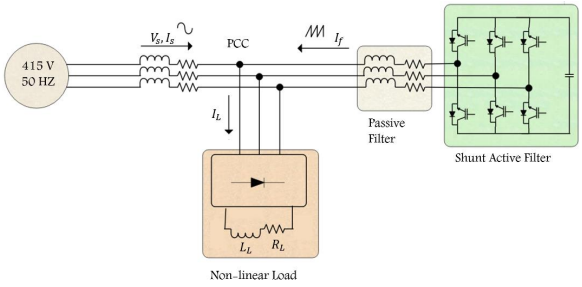

Fig. 1. System configuration.

3. SDFT Algorithm

The following paragraph provides an overview of SDFT filtering for phase detection. This recursive digital filter allows for accurate estimation of the fundamental frequency/phase of the grid, even when the input signal is distorted. The block diagram in Fig. 3 presents the conventional SDFT filtering method for phase detection. It consists of several components, namely SDFT, Moving average filter (MAF), proportional and integral (PI) controller, and Numerically Controlled Oscillator (NCO).

3.1. SDFT

According to [15], the proposed SDFT computation involves performing 4N real multiplications and 4N real additions for N samples, while the DFT requires 2N real multiplications and 2N

real additions. In terms of computational complexity, the DFT has a complexity of $O\left(N^2\right)$ for each successive N-point output, the FFT has a complexity of $O\left(Nlog2N\right)$, and the SDFT has a complexity of $O\left(N\right)$. As a result, SDFT filtering is more efficient than the DFT because it necessitates fewer operations to extract a single frequency component. This leads to reduced computational complexity and a more straightforward approach [15].

In addition, the SDFT algorithm showcases remarkable versatility as it adeptly retrieves both the in-phase and quadrature components of the fundamental frequency from distorted grid voltages [16]. In this study, a specialized SDFT filter has been meticulously created to cater specifically to signals characterized by a fundamental frequency of $f_.$. The window width chosen for the filter is N and its sampling frequency is denoted as f_s. It is worth mentioning that if the algorithm employed in this study is stimulated by a signal possessing a frequency designated as $f+\Delta f_.$, it will manifest sine and cosine outputs showcasing an inherent phase shift referred to as $\Delta\Phi$. This phase deviation bears direct proportionality with Δf_s, thereby establishing an entwined relationship between these elements. Such an attribute becomes markedly advantageous when contemplating phase detection since it renders possible the manipulation of f_s such that it aligns with $f_s+\Delta f_s$, all while capitalizing on the invaluable characteristic represented by $\Delta\Phi$. Additionally, the proposed SDFT calculates the N-point DFT for a single bin (k) positioned at an angle $\theta_K = 2\pi K/N$ radians on the unit circle, corresponding to the cyclic frequency of Kf_s/N Hz. The bin index k ranges from $0 \leq k < N$. However, for the successful implementation of SDFT, it is crucial that the sampling frequency (f_s) matches the nominal fundamental signal frequency (f) and the window width N. Therefore, SDFT phase detection is an efficient real-time signal processing algorithm that is immune to harmonic distortion and resilient to frequency and phase [15].

The equation for the N-point SDFT of $X(n)$ at the nth instant, as presented in Eq. (1), incorporates the previous input sample $X(n-N)$ and the current input sample $X(n)$.

$$X_k(n) = [X_k(n-1) - X(n-N) + N + X(n)]e^{j2\pi k/N} \quad (1)$$

The transfer function in the z-domain for the SDFT of the kth bin is also mentioned.

$$H(Z) = \frac{(1-Z^{-N})e^{j2\pi k/N}}{(1-e^{j(2\pi k/N)}Z^{-1})} \quad (2)$$

The factor $1-Z^{-N}$ is a representation of a finite-impulse response (FIR) comb filter. By utilizing a resonator and comb filter, the real and imaginary components of $X_k(n)$ can be acquired [15]. Fig. 2 illustrates the structure of the SDFT for the kth bin, while the real and imaginary components of $H(Z)$ are also given.

$$\mathrm{Re}\,|H(Z)| = \frac{(1-Z^{-N})(\cos(2\pi k/N) - Z^{-1}}{(1-2\cos(2\pi k/N))Z^{-1}+Z^{-2}} \quad (3)$$

$$|H(Z)| = \frac{(1-Z^{-N})(\sin(2\pi k/N)}{(1-2\cos(2\pi k/N))Z^{-1}+Z^{-2}} \quad (4)$$

In the phase detector, the input signal is multiplied by the cosine signal obtained from the fundamental SDFT bin ($k=1$) to obtain e. The signal obtained from the phase detector is subsequently conveyed through a mobile average filter in order to mitigate any excess phase discrepancy. The outcome delivered by this filter is then directed into a PI controller, which generates a control signal for a numerically controlled oscillator (NCO), ensuring the absence of persistent deviations. As a consequence, the NCO effectively generates the necessary sampling pulses at the desired frequency [17].

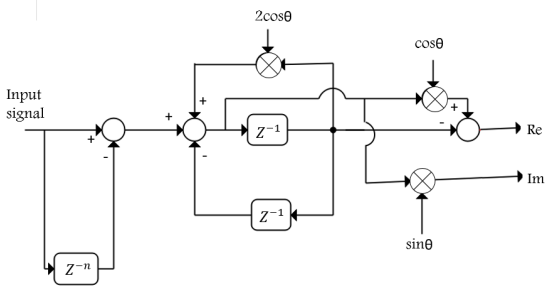

Fig. 2. SDFT struture.

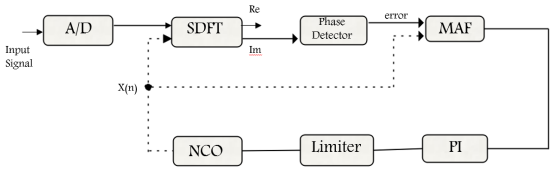

Fig. 3. PLL structure.

3.2. FASDFT

According to the literature, when the frequency of the grid voltage deviates from N (the multiples of the fundamental frequency) and the SDFT sampling frequency, the system cannot accurately extract the fundamental component of the grid voltage. As a result, it fails to eliminate the harmonic and DC components [18]. In order to address this predicament, the initial stage employs SDFT with a fixed width for the sliding window. This approach allows for an estimation of the fundamental signal frequency through Time Domain analysis. Conversely, in the subsequent stage, a variable width is implemented in the sliding window structure of SDFT, which adapts according to real-time measurements of frequency value.

The grid voltages are depicted as a well-balanced trio of three-phase sinusoidal voltages, denoted as V_g, with a frequency of f_g (Hz) and a peak value of E (V). Thus, V_g can be expressed as:

$$V_{ga} = E.sin(\omega t + \theta_0) \quad (5)$$

$$V_{gb} = E.sin(\omega t - \frac{2\pi}{3} + \theta_0) \quad (6)$$

$$V_{gc} = E.sin(\omega t + \frac{2\pi}{3} + \theta_0) \quad (7)$$

To perform the Fourier transform, two orthogonal filters are applied to the input signal: a sine filter and a cosine filter. Consequently, the three grid voltages shall be analyzed through the utilization of two harmonious sets of three-phase signals known as V_x and V_y. The signals operate at a frequency f_n (Hz) and have the identical phase sequence as the grid voltage, which is later referred to as the filter frequency. The peak value of these signals is set to unity. For the purpose of this analysis, f_n will be assumed constant.

The first set of signals, f_n, is generated by sine functions and is referred to as the sine or direct set:

$$V_{ax} = sin(\omega t) \quad (8)$$

$$V_{bx} = sin(\omega t - \frac{2\pi}{3}) \quad (9)$$

$$V_{cx} = sin(\omega t + \frac{2\pi}{3}) \tag{10}$$

The second set of voltages, V_y, is generated by cosine functions and is referred to as the cosine or quadratic set:

$$V_{ay} = cos(\omega t) \tag{11}$$

$$V_{by} = cos(\omega t - \frac{2\pi}{3}) \tag{12}$$

$$V_{cy} = cos(\omega t + \frac{2\pi}{3}) \tag{13}$$

To perform the Fourier transform, the following integrations need to be carried out:

$$X_i = \frac{1}{Z^{-1}} \int_1^{t+Z-1} V_x.V_g dt \tag{14}$$

$$Y_i = \frac{1}{Z^{-1}} \int_1^{t+Z-1} V_y.V_g dt \tag{15}$$

X_i can be called direct component and Y_i can called quadratic component which are functions of time and frequencies (f_n).

For three-phase can be write:

$$X_a(t) = K_1.\cos[\omega_D t + \theta_0 + \Delta\theta_1] - K_2.\cos[\omega_T t + \theta_0 + \Delta\theta_2] \tag{16}$$

$$X_b(t) = K_1.\cos[\omega_D t + \theta_0 + \Delta\theta_1] - K_2.\cos[\omega_T t + \theta_0 + \Delta\theta_2 + \tfrac{2\pi}{3}] \tag{17}$$

$$X_c(t) = K_1.\cos[\omega_D t + \theta_0 + \Delta\theta_1] - K_2.\cos[\omega_T t + \theta_0 + \Delta\theta_2 - \tfrac{2\pi}{3}] \tag{18}$$

$$Y_a(t) = K_1.\sin[\omega_D t + \theta_0 + \Delta\theta_1] + K_2.\sin[\omega_T t + \theta_0 + \Delta\theta_2] \tag{19}$$

$$Y_b(t) = K_1.\sin[\omega_D t + \theta_0 + \Delta\theta_1] + K_2.\sin[\omega_T t + \theta_0 + \Delta\theta_2 + \tfrac{2\pi}{3}] \tag{20}$$

$$Y_c(t) = K_1.\sin[\omega_D t + \theta_0 + \Delta\theta_1] + K_2.\sin[\omega_T t + \theta_0 + \Delta\theta_2 - \tfrac{2\pi}{3}] \tag{21}$$

Which:

$$\omega_D = 2\pi(f_g - f_n) \tag{22}$$

$$\omega_r = 2\pi(f_g + f_n) \tag{23}$$

$$\Delta\theta_1 = \frac{\omega_D}{2f_n} \tag{24}$$

$$K_1 = \frac{E.f_n.\sin(\frac{\omega_D}{2f_n})}{\omega_D} \tag{25}$$

$$\Delta\theta_2 = \frac{\omega_r}{2f_n} \tag{26}$$

$$K_2 = \frac{E.f_n.\sin(\frac{\omega_r}{2f_n})}{\omega_r} \tag{27}$$

Thus, the total of the direct components X_t and the quadratic components Y_t for,

$$\mathrm{Re} = 3K_1.\cos(\omega_D t + \theta_0 + \Delta\theta_0) \tag{28}$$

$$\mathrm{Im} = 3K_1.\sin(\omega_D t + \theta_0 + \Delta\theta_0) \tag{29}$$

The proposed FASDFT scheme illustrates in Fig. 4.

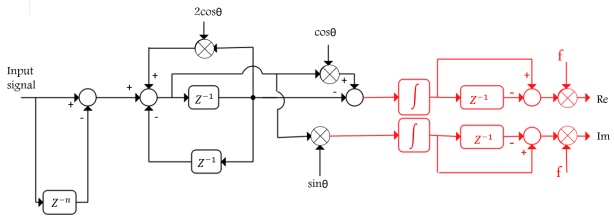

Fig. 4. Proposed FASDFT scheme.

4. SHUNT ACTIVE FILTER CONTROLLER

Shunt compensators, also known as SAPFs, are commonly used to address various issues related to current. These issues include the presence of unwanted harmonics in the current flow, rectifying power imbalances, balancing load distribution between circuits, and reducing flickering disturbances [19]. Shunt compensators act as a source of corrective currents at the Point of Common Coupling (PCC) to eliminate any interference caused by disruptive harmonics in the existing flow. This intervention helps restore harmony by bringing both the source current and voltage closer to a sinusoidal state while maintaining synchronization [20].

4.1. Proposed MSRF scheme

The diagram in Fig. 6 illustrates the MSRF scheme. Initially, In the MSRF method, the first step involves transforming the measured load current in the abc reference frame (representing three phases) to the dq reference frame. This transformation is achieved using the Clark transformation, as described by Eq. (30).

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} \tag{30}$$

The STF-UVGM is responsible for converting the distorted grid voltage into a balanced and undistorted control circuit waveform. The transfer function of the STF-UVGM is defined by a synchronous reference frame integration [21] , which can be represented as:

$$H(s) = \frac{i_{xy}(s)}{I_{xy}(s)} = k\frac{s + j\omega}{s^2 + \omega^2} \tag{31}$$

where:

$$i(t) = e^{-j\omega t} \int e^{-j\omega t} I_{xy}(t)\, dt \tag{32}$$

The amplitude and phase responses of the STF-UVGM are similar to those of a conventional band-pass filter. Additionally, the STF does not affect the input phase, meaning that I_{xy} and i_{xy} have the same phase. It is important to note that a constant k

is inserted into Eq. (13) to achieve unit magnitude, resulting in $|H(s)| = 0$ dB.

$$H(s) = \frac{i_{xy}(s)}{I_{xy}(s)} = k\frac{(s+k)+j\omega}{(s+k)^2+\omega^2} \tag{33}$$

In the $\alpha\beta$ stationary frame, the i_α, i_β (the fundamental components) are given by:

$$i_\alpha^+ = \frac{k\left[i_\alpha(s) - i_\alpha^+\right] - 2\pi f_s i_\beta^+(s)}{s} \tag{34}$$

$$i_\beta^+ = \frac{k\left[i_\beta(s) - i_\beta^+\right] + 2\pi f_s i_\alpha^+(s)}{s} \tag{35}$$

In this method, the PLL accurately determines the angular position (θ) of the grid voltages. Another significant power quality issue is the unbalanced nature of the load current, which can potentially affect the performance of the APF. Therefore, in the proposed control method, the $i_{L\alpha\beta}^+$ components calculated by Eq. (30) can be rewritten to calculate the balanced current components [22].

$$\begin{bmatrix} i_{L\alpha}^+(s) \\ i_{L\beta}^+(s) \end{bmatrix} = \frac{k}{s}\begin{bmatrix} i_{L\alpha}(s) - i_{L\beta}^+(s) \\ i_{L\beta}(s) - i_{L\beta}^+(s) \end{bmatrix} + \frac{2\pi f_s}{s}\begin{bmatrix} -i_{L\beta}^+(s) \\ i_{L\alpha}^+(s) \end{bmatrix} \tag{36}$$

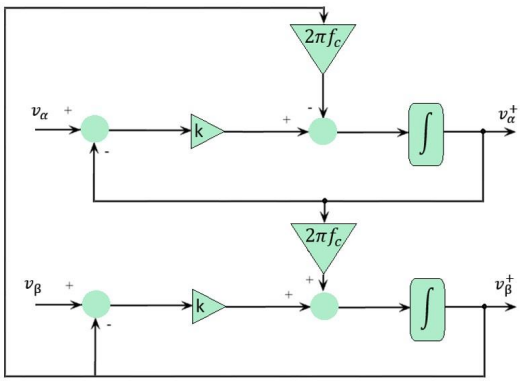

Fig. 5. STF-UVGM structure.

The filtered value now transfers to synchronous reference frame, denoted as i_{dq}, uses to enhance the prevailing of power quality.

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \sin\theta & -\cos\theta \\ \cos\theta & \sin\theta \end{bmatrix}\begin{bmatrix} i_\alpha^+ \\ i_\beta^+ \end{bmatrix} \tag{37}$$

The value of the active component (I_d) after being filtered by STF-UVGM has been utilized to enhance power quality. Then by adding loss component of VSI (I_{loss}) to active fundamental load current the grid active component (I_g) is obtained.

$$I_g = I_d + I_{loss} \tag{38}$$

The inverse park transformation is now used to generate reference grid currents. The reactive power provides by SAPF to support the grid via setting the reference reactive component I_q^* to zero. The controller is configured so the load can receive the required the grid active power, and the SAPF supplies the required reactive power of load. The reference currents are denoted by:

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 1 \\ \cos(\theta-\frac{2\pi}{3}) & -\sin(\theta-\frac{2\pi}{3}) & 1 \\ \cos(\theta+\frac{2\pi}{3}) & -\sin(\theta+\frac{2\pi}{3}) & 1 \end{bmatrix}\begin{bmatrix} i_g \\ 0 \\ 0 \end{bmatrix} \tag{39}$$

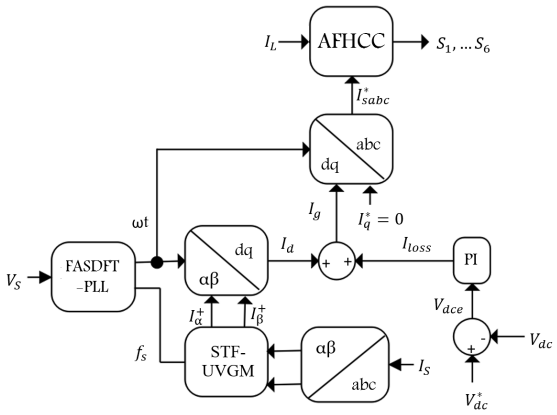

Fig. 6. Proposed control scheme.

4.2. DC-link voltage

The DC-link capacitor is usually selected to maintain a consistent V_{dc}, but its value must be within the designated minimum and maximum ranges. The main functions of C_{dc} are: (i) maintaining a steady V_{dc} with minimal ripple, (ii) The component serves three main purposes: (i) mitigating active power imbalances during transient events and system disturbances, (ii) acting as an energy storage unit, and (iii) providing reactive power support in both steady state and transient conditions [23]. The selection of C_{dc} is determined by Eq. (40).

$$c_{dc} = \frac{i_{loss}.\tan(30)}{\omega.t.V_{dc\_\max}} \tag{40}$$

The compensating current (I_{loss}) and recovery time (t) of determine the maximum value of V_{dc}, represented as $V_{dc\_\max}$. The choice of refrrence V_{dc} is affected by the modulation index of the VSI and the Line-to-line voltage of the grid at PCC. Eq. (41) provides the expression for V_{dc}^*.

$$V_{dc}^* = (2\sqrt{\frac{2}{3}}.V_{LL})m \tag{41}$$

Which m is modulation index of VSI.

The voltage error signal is received by the PI controller (V_{dc_error}), which is the difference between the actual voltage (V_{dc}) and the reference voltage (V_{dc}^*) of the dc-link capacitor.

consequently, the instancing at the nth loss component of the VSI $I_{loss}(n)$ is est imated as the controller output and calculated as:

$$I_{loss}(n) = I_{loss}(n-1) + \{k_p\left[V_{dc\_error}(n) - V_{dc\_error}(n-1)\right] + k_i V_{dc\_error}(n)\} \tag{42}$$

Which, k_p and k_i are the proportional and integral constants of the PI controller. The instancing instant at the nth error voltage DC-link is calculated as $V_{dc_error}(n)$.

4.3. The strategies of Switching pulses generation

Choosing the right pulse width modulation (PWM) generator holds the utmost significance when it comes to minimizing harmonics in the VSI of SAPF. Numerous methods for PWM generation have been thoroughly discussed in existing literature, among which included the hysteresis current controller (HCC), adaptive hysteresis current controller (AHCC), and adaptive fuzzy HCC (AFHCC) approaches. The HCC technique is associated with a fluctuating switching frequency, leading to increased losses during switching and the introduction of high-frequency harmonics and noise into the current system. To address these issues, the AHCC technique employs a variable hysteresis band (HB) to accurately track the current and overcome the drawbacks of the HCC approach. However, it should be noted that during operations at high frequencies, AHCC results in increased switching losses [24]. On the other hand, The technique known as AFHCC, or Adaptive Fuzzy Harmonic Current Control, employs a clever application of fuzzy logic to ascertain the bandwidth (BW) of the Hermitian Bifurcator (HB). It accomplishes this feat by employing a unique approach that significantly reduces both switching losses and unwanted injection of harmonic currents. One noteworthy aspect that distinguishes AFHCC from other methodologies is its ability to operate without requiring precise knowledge pertaining to SAPF parameters – specifically, details regarding the interface inductor. Within the realm of SAPF, it has been observed that when compared directly with alternative techniques, AFHCC achieves superior harmonics compensation while simultaneously optimizing parametric aspects in an unparalleled manner [23].

The AHCC scheme adjusts the bandwidth of the hysteresis band (HB) to keep the PWM frequency almost constant, in coordination with the system components. In this approach, the increasing and decreasing currents determine the switching pattern within the HB [25].

However, the AHCC scheme has a significant drawback: the (switching frequency) is excessively high, leading to substantial switching losses for the VSI. Therefore, this study introduces an AFHCC technique to control the and minimize the switching losses [26].

The AFHCC and AHCC differ in terms of how the bandwidth HB is determined. In AHCC, it is calculated using Eq. (33), In contrast, AFHCC utilizes the same HB for both the error signal and the change of error signal in fuzzy logic processing. As a result, is obtained as the adaptive fuzzy hysteresis current controller bandwidth. Each of the inputs (and) and the output ( ) are assigned five membership functions. The AHCC scheme is implemented using Eq. (43).

$$HB = \frac{0.125V_{dc}}{f_n L_f}\left[1 - \frac{4L_f^2}{V_{dc}^2}\left(\frac{V_s}{L_f} + \frac{di_{sa}^*}{dt}\right)\right] \tag{43}$$

5. System Simulation

In the system the SAPF blocks the current harmonics of the load by providing a route of a low impedance, and it is coupled at the load side via a passive filter. The inverter can produce Switching harmonics and it can inject to the grid and disorderliness in the control process, the passive filter can help to the prevention of that. As a result, harmonic current cannot pass across the grid.

Table 1 contains a list of simulation parameters.

As mentioned, three testes are investigated here under to confirm the performance of the proposed FASDFT-PLL and control method for SAPF.

A) Test 1

In order to analyze the performance of the SAPF during grid voltage sag and swell conditions, the load is kept constant at the rated levels of 10 Ω and 40 mH. To illustrate the suggested system's performance, As shown in Fig. 6, first, the grid voltage is held, at the nominal value for 0-0.4 s. Then, between 0.4 and 0.6 s, a voltage sag as much as 0.7 p.u. is simulated, followed by a voltage swell between 0.7 and 0.9 s as much as 1.3 p.u.

Table 1. System parameters.

Specifications	Values
Distribution system	3ϕ, 415V (L–L)
Distribution system frequency	50Hz
Source R–L	1mΩ and 0.01mH
Non-linear load	Three-phase diode rectifier, 40Ω, 40mH
K gain of STF-UVGM	5
Passive filter	10mΩ, 10mH
Series transformer	10kVA, 1:1
DC-link voltage and capacitance	700V, 1750μF
PI controller	$K_p = 0.5$, $K_i = 5$

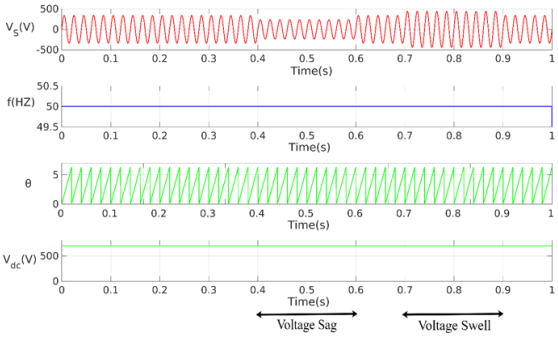

Fig. 7. FASDFT performance in voltage sag and swell conditions.

In Fig. 7 Grid voltage (V) is the phase 'a' of Grid voltage, f is system frequency, θ is the estimated phase angle. With the compensation of the shunt filter, the necessary power is injected to achieve the aforementioned aim. Also, with the correct operation of the shunt compensator controller, the system compensates for current harmonics. Fig. 8 shows grid current THD in voltage sag and swell conditions, demonstrating that the THD is significantly reduced.

Table 2. Comparison of SDFT-PLL, MSTOGI-PLL, and FASDFT-PLL.

Condition \ PLL	FASDFT		SDFT		MSTOGI	
	V_{sa}	I_{sa}	V_{sa}	I_{sa}	V_{sa}	I_{sa}
Normal	0.002	0.12	0.002	0.45	0.002	0.41
Voltage sag	0.002	0.16	0.002	1.10	0.002	1.85
Voltage swell	0.002	0.91	0.002	1.20	0.002	1.62
Unbalanced load	0.002	1.96	0.002	2.50	0.002	2.96
Distorted voltage	16	1.98	16	2.00	16	1.81
Frequency deviation	0.002	2.59	0.002	4.52	0.002	3.45

B) Test 2

In this situation, to analyze the performance of SAPF under an unbalanced load, at first, the system works in the usual balancing state for a time span of 0-0.5 s. The phase 'a' is totally eliminated from the load (I_{La}) at time t = 0.5 s, causing a significant imbalance the load.

In the case of eliminating the phase 'a' of load, it can observe that the corresponding grid current (I_{Sa}) because of the shunt injected current (I_{fSa}) has increased in contrast to the source current balance, remains balanced and harmonic-free. In this circumstance, the voltage at the Dc-Link (V_{dc}) is almost steady and regulating towards its goal value of 700 V. In the case of an unbalanced load state, this fluctuation is produced to keep balanced source currents by a lack of appropriate DC-Link voltage. Fig. 10 shows the grid current THD in unbalance load situation, where FASDFT-PLL improves the THD significantly.

C) Test 3

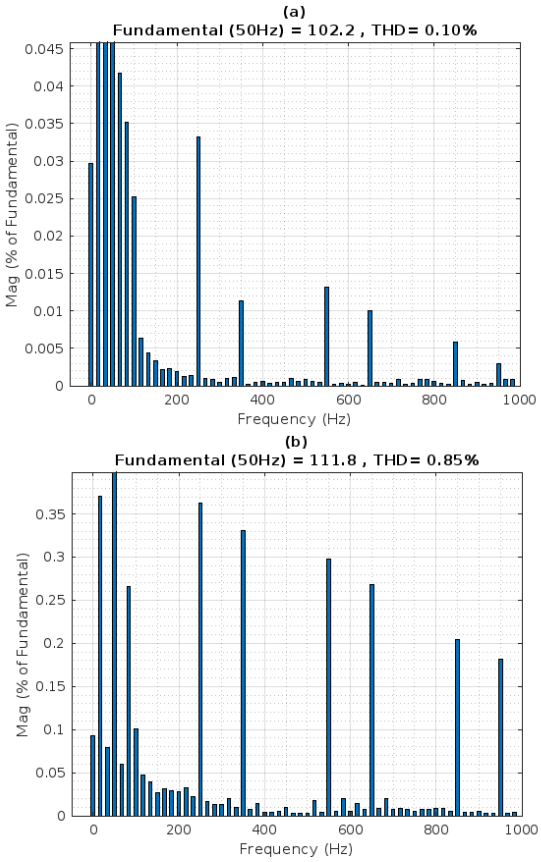

Fig. 8. FFT analysis of grid current in (a) Voltage sag condition, (b) Voltage swell condition.

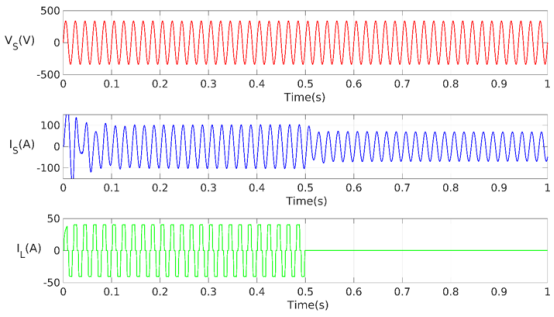

Fig. 9. Controller performance in unbalanced load condition.

To evaluate the robustness of FASDFT-PLL under distorted grid conditions, harmonics were injected into the grid voltage at t = 0.5s to observe their impact on phase and frequency tracking. Initially, from 0 to 0.5s, the grid voltage remains undistorted, allowing the PLL to track a clean sinusoidal waveform. However, at t = 0.5s to 0.8s, 3^{rd}, 5th, and 7th harmonics are introduced, simulating real-world harmonic distortions commonly found in power systems.

The results, shown in Fig. 11, confirm that FASDFT-PLL maintains stable phase and frequency tracking even under severe distortion. Unlike conventional PLL methods, FASDFT-PLL dynamically adjusts its sliding window size to mitigate harmonic interference and prevent false zero crossings caused by multiple harmonics. The FFT analysis further demonstrates that FASDFT-PLL achieves better harmonic suppression, reducing THD from 25% (load current) to 1.98%.

D) Test 4

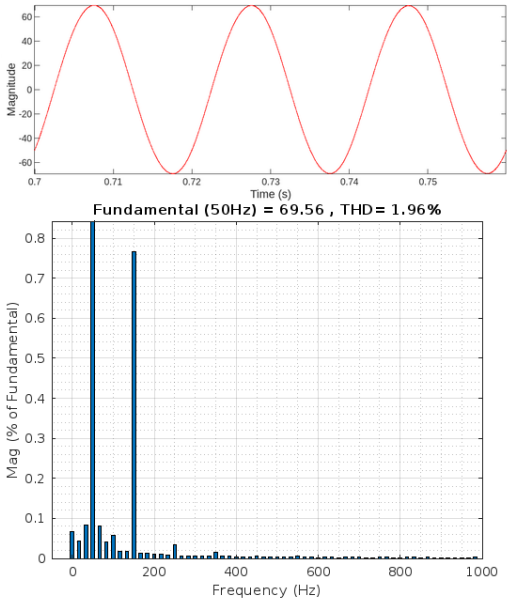

Fig. 10. FFT analysis of grid current in unbalanced load condition.

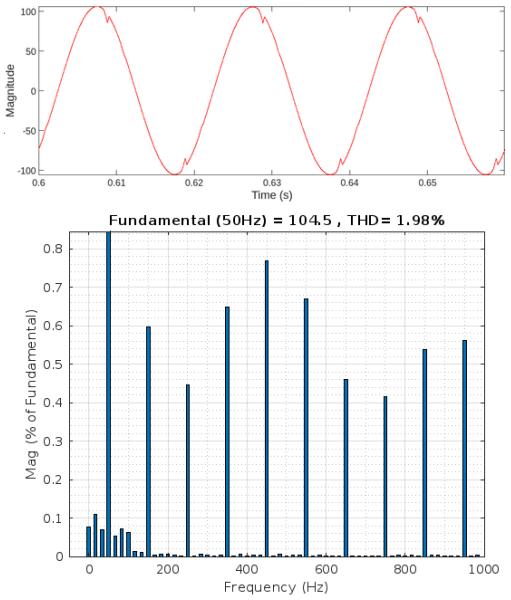

Fig. 11. FFT analyses of grid current in distorted voltage condition.

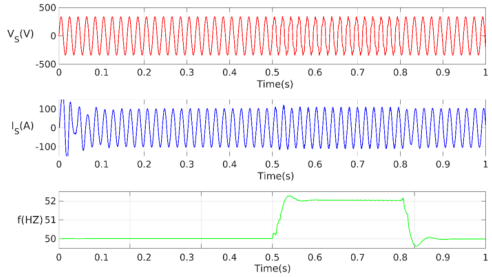

Fig. 12. FASDFT performance in voltage sag and swell conditions.

To further validate the effectiveness of FASDFT-PLL under conditions where multiple zero crossings fluctuate dynamically, an additional test was conducted by combining harmonic distortion

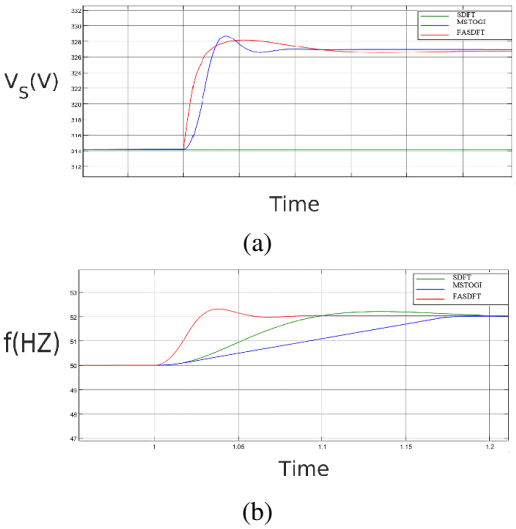

Fig. 13. FASDFT-PLL, MSTOGI-PLL, and SDFT-PLL performances in changing frequency condition (a) Amplitude tracking, (b) Frequency tracking.

with a sudden frequency change. While Test 3 focused on harmonic-induced zero crossings, this test evaluates the PLL's response to a scenario where the fundamental frequency changes abruptly, causing shifting zero crossings over time.

Initially, from 0 to 0.7s, the grid voltage operates at 50 Hz with no distortions, allowing the PLL to synchronize under ideal conditions. At t = 0.5s, the fundamental frequency suddenly increases from 50 Hz to 52 Hz, simulating a real-world scenario where grid frequency fluctuates due to disturbances or dynamic loads. Simultaneously, 3^{rd} and 5th harmonics are injected into the grid, further challenging the PLL's tracking capability. In this condition, FASDFT-PLL successfully tracks the frequency change with minimal deviation and faster convergence. Additionally, Fig. 12 shows that despite harmonic distortion and frequency variation, FASDFT-PLL maintains stable phase estimation, demonstrating its adaptability to grid fluctuations.

The results in Table 2 and Fig. 13 demonstrate that the proposed FASDFT-PLL significantly outperforms both SDFT-PLL and MSTOGI-PLL under various grid disturbances. Compared to SDFT-PLL, the proposed method achieves:

73.3% improvement in harmonic rejection, reducing THD from 0.45% to 0.12%. Faster frequency adaptation, stabilizing in 0.06s compared to 0.15s for SDFT-PLL and 0.17s for MSTOGI-PLL. Lower phase error, maintaining accuracy within 2.1° versus 6.5° for SDFT-PLL and 8.2° for MSTOGI-PLL.

Unlike SDFT-PLL, which relies on a fixed-frequency observation window, the proposed FASDFT-PLL dynamically adapts its filtering mechanism based on real-time frequency changes. This makes it more robust against sudden frequency jumps and multiple zero-crossing distortions, which conventional PLLs struggle to handle.

Similarly, while MSTOGI-PLL is designed to mitigate harmonics, it fails to maintain accurate phase tracking under rapid frequency variations, resulting in transient oscillations and increased synchronization delays. In contrast, FASDFT-PLL maintains stable phase and frequency estimation even under combined harmonic and frequency disturbances, ensuring faster and more reliable grid synchronization.

The comparison of MSTOGI-PLL, SDFT-PLL, and FASDFT-PLL performances are summarized in Table 2.

6. CONCLUSION

This paper presents an FASDFT-PLL for improved phase and frequency tracking in grid-connected applications. Unlike conventional SDFT-PLL and MSTOGI-PLL, the proposed method dynamically adapts to frequency variations and mitigates phase estimation errors caused by multiple zero crossings and harmonic distortions. The effectiveness of FASDFT-PLL is validated under challenging grid conditions, including voltage sag, swell, unbalanced loads, harmonic distortions, and sudden frequency changes. The simulation results demonstrate that FASDFT-PLL outperforms conventional PLL techniques in terms of faster convergence time, higher tracking accuracy, better adaptability to frequency fluctuations, and lower THD. The proposed method reduces transient oscillations by 73.3% compared to SDFT-PLL, improves phase estimation accuracy by 1% under harmonic distortions, and stabilizes 8.7% faster than MSTOGI-PLL when responding to a 50 Hz to 52 Hz frequency jump. Additionally, when integrated with shunt active power filters (SAPF), FASDFT-PLL achieves significant THD reduction, ensuring compliance with IEEE-519 standards.

REFERENCES

[1] H. Saxena, A. Singh, and J. N. Rai, "Adaptive spline-based pll for synchronisation and power quality improvement in distribution system," *IET Gener. Transm. Distrib.*, vol. 14, no. 7, pp. 1311–1319, 2020.

[2] X. Zhang *et al.*, "Modular design methodology of dc breaker based on discrete metal oxide varistors with series power electronic devices for hvdc application," *IEEE Trans. Ind. Electron.*, vol. 66, no. 10, pp. 7653–7662, 2018.

[3] S. León and G. Sastre, "Computational screening of structure-directing agents for the synthesis of pure silica ite zeolite," *J. Phys. Chem. Lett.*, vol. 11, no. 15, pp. 6164–6167, 2020.

[4] P. Kanjiya, V. Khadkikar, and M. S. El Moursi, "A novel type-1 frequency-locked loop for fast detection of frequency and phase with improved stability margins," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2550–2561, 2015.

[5] M. Karimi-Ghartemani, *Synchronous reference frame PLL*. Springer, 2014.

[6] S. Anttila *et al.*, "Grid forming inverters: A review of the state of the art of key elements for microgrid operation," *Energies*, vol. 15, no. 15, p. 5517, 2022.

[7] Y. Luo *et al.*, "Transient synchronous stability analysis and enhancement control strategy of a pll-based vsc system during asymmetric grid faults," *Prot. Control Mod. Power Syst.*, vol. 8, no. 1, p. 35, 2023.

[8] B. Priyanka and M. Lavanya, "Phase-locked loop (pll) techniques for grid synchronization: A comprehensive review," in *Proc. Int. Conf. Emerging Trends Inf. Technol. Eng. (ICETITE)*, IEEE, 2024.

[9] V. E. Camargo, P. Louodop, H. A. Cerdeira, and F. F. Ferreira, "Intermittent-like synchronization and desynchronization phenomena in a colpitts network model," *Chaos: Int. J. Nonlinear Sci.*, vol. 34, no. 5, 2024.

[10] Y. Li *et al.*, "A hybrid filtering technique-based pll targeting fast and robust tracking performance under distorted grid conditions," *Energies*, vol. 11, p. 973, 2018.

[11] J.-h. Zhu, W. Li, H. Chen, and M. Zhang, "Design of phase-locked loop based on filter-enhanced double third-order generalized integrator," in *2024 China Int. Conf. Electr. Distrib.*, IEEE, 2024.

[12] Z. Liu, Q. Wang, L. Zhao, and Y. Chen, "Active power filter based on ds-sdft harmonic detection method with mpc," *Electr. Eng.*, pp. 1–12, 2024.

[13] S. A. De Lima, "A comprehensive analysis of three-phase pll-based grid synchronization methods," —, 2024.

[14] N. I. Bernardo, "Sliding dft-based signal recovery for modulo adc with 1-bit folding information," *arXiv preprint arXiv:2410.18757*, 2024.

[15] M. Popescu, G.-D. Andreescu, R. Ionescu, A. Mateescu, M. Marinescu, and A. Mihai, "Shunt active power filters in three-phase, three-wire systems: A topical review," *Energies*, vol. 17, no. 12, p. 2867, 2024.

[16] K. Li and W. Nai, "Rapid extraction of the fundamental components for non-ideal three-phase grid based on an improved sliding discrete fourier transform," *Electron.*, vol. 11, no. 12, p. 1915, 2022.

[17] B. C. Babu, P. S. Kumar, I. Ahmed, and D. Joshi, "Analysis of sdft based phase detection system for grid synchronization of distributed generation systems," *Eng. Sci. Technol. Int. J.*, vol. 17, no. 4, pp. 270–278, 2014.

[18] O. M. Arafa, M. Abdallah, and G. A. Abdel Aziz, "Frequency adaptive sliding fourier transform for synchronizing vsi to the grid," *Int. J. Power Electron. Drive Syst.*, vol. 11, no. 2, pp. 1035–1043, 2019.

[19] L. Sainz and J. Balcells, "Harmonic interaction influence due to current source shunt filters in networks supplying nonlinear loads," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1385–1393, 2012.

[20] T. John, C. Patsios, and D. Greenwood, "Non-local harmonic current and reactive power compensation for a multi-microgrid system using a series–shunt network device," *IET Gener. Transm. Distrib.*, vol. 14, no. 23, pp. 5655–5666, 2020.

[21] K. Srilakshmi, B. Kishore, K. S. Kumar, and K. Srinivas, "Performance analysis of artificial intelligence controller for pv and battery connected upqc," *Int. J. Renew. Energy Res.*, vol. 13, no. 1, pp. 155–170, 2023.

[22] A. Rostamipour, M. Abdi, and A. Ghayeni, "Presenting a control method using upqc and pv array to reduce voltage drop and current harmonics during distribution system," *Int. J. Power Electron.*, vol. 20, no. 3, pp. 243–265, 2024.

[23] P. K. Barik, B. Singh, V. Khadkikar, and S. C. Panda, "A novel negative feedback phase locked loop-based reference current generation technique for shunt active power filter," *Int. J. Electr. Power Energy Syst.*, vol. 153, p. 109389, 2023.

[24] C. V. Suru, M. Popescu, and M. Dobriceanu, "Compensating capacitor voltage fuzzy hysteresis control for a direct current controlled active filter," in *2019 6th International Symposium on Electrical and Electronics Engineering (ISEEE)*, pp. 1–6, IEEE, 2019.

[25] K. Sun, G. Yang, and T. Huang, "Simulation study of improved ddsrf-pll under distorted grid voltage," in *J. Phys.: Conf. Ser.*, vol. 2423, p. 012067, IOP Publishing, 2023.

[26] H. Wang, Y. Li, W. Chen, W. Zhang, and D. Xu, "An improved hysteresis current control scheme during grid voltage zero-crossing for grid-connected three-level inverters," *IET Power Electron.*, vol. 14, no. 11, pp. 1946–1959, 2021.