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*Research Paper*

# Transformer-Less Voltage Boosting Switched-Capacitor Inverter for PV Application

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***Abstract***— *This study proposes a single-phase switched-capacitor (SC) topology that eliminates the need for a transformer and incorporates a shared ground. The topology utilizes eleven switches, one diode, and three capacitors to generate a nine-level waveform. The key attributes of the proposed design include zero leakage current(LC), voltage boosting capability, reduced voltage stress, and self-balancing of capacitor voltage. Furthermore, there is no need for extra balancing circuits or sensors to ensure the equilibrium of capacitor voltages. A comprehensive examination of the circuit description and operating principle has also been conducted. Through a concise comparison, the proposed topology has been shown to outperform existing alternatives in terms of component count, voltage stress, and gain. The utilization of the Simulation environment ensures the accuracy of the theoretical concept.*

***Keywords***—Common-mode voltage, leakage current, multi level inverter, transformerless inverter, voltage gain.

## 1. INTRODUCTION

In the past two decades, photovoltaic generation has become increasingly significant in addressing electricity demand. Photovoltaic (PV) systems offer appealing characteristics such as stability, reliability, eco-friendliness, and competitiveness compared to both conventional and non-conventional energy sources [1], [2].

An on-grid PV system need a converter because the PV system's output voltage is direct voltage. The issue may arise owing to dangerous voltage, which can be avoided by providing a grid-tied inverter. There are two types of grid-tied inverters: those that utilize a transformer, and those that do not require a transformer, known as transformer-based inverters and transformer-less inverters, respectively. The transformer-basedinverter maintains galvanic shielding between the grid and PV cells. It, therefore, provides greater security. However, a transformer adds expense, size, and inefficiency to the system.

Transformer-less inverters offer a solution to the aforementioned issues associated with transformer-based inverters.The absence of galvanic isolation between the grid and PV panel increases the likelihood of issues such as LC, ground faults, electromagnetic interference, losses, and significant protection concerns [3–5].

Fig. 1 depicts the equivalent circuit of a standard transformerless inverter, including key components like power semiconductor switches, output filters, ground impedance, and parasitic capacitance. The existence of parasitic capacitance (CP) between the PV panel and the ground induces the flow of LC in the system. The common-mode voltage $v_{cm}$ and the differential mode $v_{dm}$ are defined according to [1].

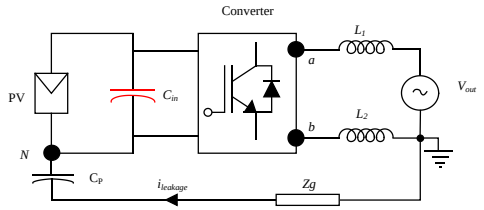


Fig. 1. Typical transformerless topology.

$$v_{cm} = \frac{(v_{aN} + v_{bN})}{2} \tag{1}$$

$$v_{dm} = (v_{aN} - v_{bN}) \left( \frac{L_2 - L_1}{2\,(L_1 + L_2)} \right) \tag{2}$$

where $v_{aN}$, $v_{bN}$ be the potential difference between the points $a$ and $b$ with respect to the point $N$ respectively. The total voltage measured in common mode can be expressed as:

$$v_{tcm} = \frac{(v_{aN} + v_{bN})}{2} + (v_{aN} - v_{bN}) \left( \frac{L_2 - L_1}{2\,(L_1 + L_2)} \right) \tag{3}$$

The LC ($i_l$) can be defined as:

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$$i_l = C_P \frac{d(v_{tcm})}{dt} \tag{4}$$

According to Eq. (4), LC can be avoided by removing parasitic capacitance or by maintaining the entire common-mode voltage. There are two distinct methods that are utilized in the transformer-less inverter in order to get rid of or cut down on the LC. These methods are (i) modified PWM technique and (ii) structural design of the topology. Modified modulation strategies for reducing LC are discussed in [3, 4]. In accordance with the structural design, three different solutions have been put into action in order to reduce or eliminate the LC [5–15]. These techniques can be grouped together into the following categories: (a) Neutral point clamped inverter; (b) Decoupling of DC/AC side; and (c) Common ground inverter.

The PV application of the neutral point clamped topology, as described in [6–10], aims to minimize LC and maintain a constant common-mode voltage. The topology [6] utilizes the full DC bus voltage to synthesize the output voltage but it has the lacks voltage boosting ability. Topologies [6, 7] consist of a larger count of switching components, and the DC-link voltage requirement is twice that of the maximum grid value. Consequently, these topologies do not effectively eliminate LC. The transformer-free inverter proposed in [8, 9] benefits from DC/AC decoupling. To avoid LC during the freewheeling period, all of these configurations rely on a full-bridge architecture and employ additional switches on either the DC side [8] or the AC side [9, 10] to provide isolation between the grid and the PV module. These topologies are more expensive, complicated, and unstable because they necessitate more switching components.

The difficulties with the last two methods described above can be avoided by adopting a common ground strategy [11–15]. To avoid LC, the negative terminal of the solar module is linked to the neutral point of the utility grid. The capacitor produces voltages with a negative polarity. The following topologies have more active and passive parts to prevent LC, which is one of their main downsides.

The paper referenced in citation [16] introduces an innovative modulation technique tailored for two-level Voltage Source Inverters (VSIs), which bears resemblance to the Space Vector Pulse Width Modulation (SVPWM) approach. However, it offers distinct vector diagram representations and dwell time computations aimed at addressing the challenges commonly encountered with the conventional SVPWM method. However, the primary limitation of the proposed solution is its inability to enhance voltage. A novel single-phase boost inverter design, as detailed in Ref. [17], eliminates the need for isolation by employing a shared terminal between its input and output ports, effectively mitigating leakage current concerns. This innovative configuration comprises three active switches, enabling voltage regulation through the adjustment of duty cycles associated with one of the switches. However, the primary disadvantage of the suggested solution is the increased voltage stress experienced by the switching component, resulting in higher design costs. In Ref. [18], a five-level MLI with two dc voltage sources, two quasi-z-sources, and five switching devices has been introduced. This structure employs several sources, resulting in a complex design. A three-phase inverter and a DC-DC power converter are the components that make up a multi-stage power generation system that is ideal for renewable energy sources [19].

The literature review's benefits and cons inspired the development of a novel transformer-less switched-capacitor (SC) topology with a single source and a common ground. The following are some of the unique aspects of the suggested topology that make it so novel:

1) The voltage of the capacitor is naturally self-regulated.
2) Eliminate the LC.
3) Reduced number of switching component.
4) Voltage stress is restricted within the supply voltage across all the switches.
5) Utilization of a single direct current source.
6) The capability of doubling the input voltage.

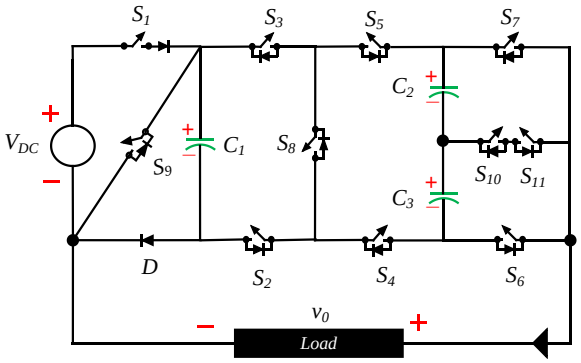



Fig. 2. Schematic diagram of the proposed single-phase common ground nine-level transformerless SC topology.

Table 1. Valid switching sequence for different voltage level.

| State | Active switch | | | | | | | | | | Effect of capacitors | $v_0 = (*V_{DC})$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $S_9$ | $S_{10}$ | $S_{11}$ | |
| A | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | $C_1\uparrow, C_2\uparrow, C_3\uparrow$ | 0 |
| B | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | $C_1\uparrow, C_2\uparrow, C_3\uparrow$ | +0.5 |
| C | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | $C_1\uparrow, C_2\uparrow$ | -0.5 |
| D | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | $C_1\uparrow, C_2\uparrow, C_3\uparrow$ | +1 |
| E | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | $C_1\uparrow, C_2\downarrow, C_3\downarrow$ | -1 |
| F | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | $C_1\uparrow, C_3\downarrow$ | +1.5 |
| G | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | $C_1\downarrow, C_2\downarrow$ | -1.5 |
| H | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | $C_1\uparrow, C_2\downarrow, C_3\downarrow$ | +2 |
| I | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | $C_1\downarrow, C_2\downarrow, C_3\downarrow$ | -2 |

The paper's organization is as follows: Section 2 presents an overview, detailing the main operation, and providing guidelines for selecting capacitance in the proposed configuration. In Section 3, the modulation scheme is discussed, followed by an exploration of loss analysis in Section 4. Section 5 provides a concise comparative analysis of existing transformer-less topologies. Section 6 presents simulation and experimental results. Finally, the paper concludes in Section 7 with a summary of the proposed topology.

## 2. PROPOSED TOPOLOGY

### 2.1. Circuit analysis

A schematic representation of a transformer-free, nine-level, single-phase, common ground topology is shown in Fig. 2. Ten power switches ($S_1 \sim S_{11}$), a diode ($D$), three capacitors ($C_1 \sim C_3$) and a DC voltage source ($V_{DC}$) comprise the circuit. Except for switch $S_1$ each switch is made up of a single IGBT with an antiparallel diode. The diode and transistor in the switch $S_1$ are connected in series. The parasitic capacitance between the PV panel and earth is effectively eliminated by directly connecting the negative terminal of the PV panel to the neutral point of the grid. This structural design ensures the prevention of LC. The design utilizes a single DC supply and three capacitors to provide nine levels ($\pm 2V_{DC}, \pm 1.5V_{DC}, \pm 1V_{DC}, \pm 0.5V_{DC}, and\ 0$). All switches' blocking voltages, with the exception of $S_{10}$, $S_{11}$, are constrained to the $V_{DC}$ input supply voltage. The input supply voltage ($V_{DC}$) is capped at 50% by the $S_{10}$, $S_{11}$, switches. Load terminals are represented by $x$ and $y$, while the load voltage is shown by $v_0$. Table 1 lists the possible switching states and their corresponding switching order. The switch positions "0" and "1" correspond to being "ON" and "OFF" accordingly. The effects of charging and discharging capacitors are represented by the symbols "↑" and "↓" respectively. The red and blue dashed lines in each state represent the simulated voltage level and the charging path of the capacitors, respectively.

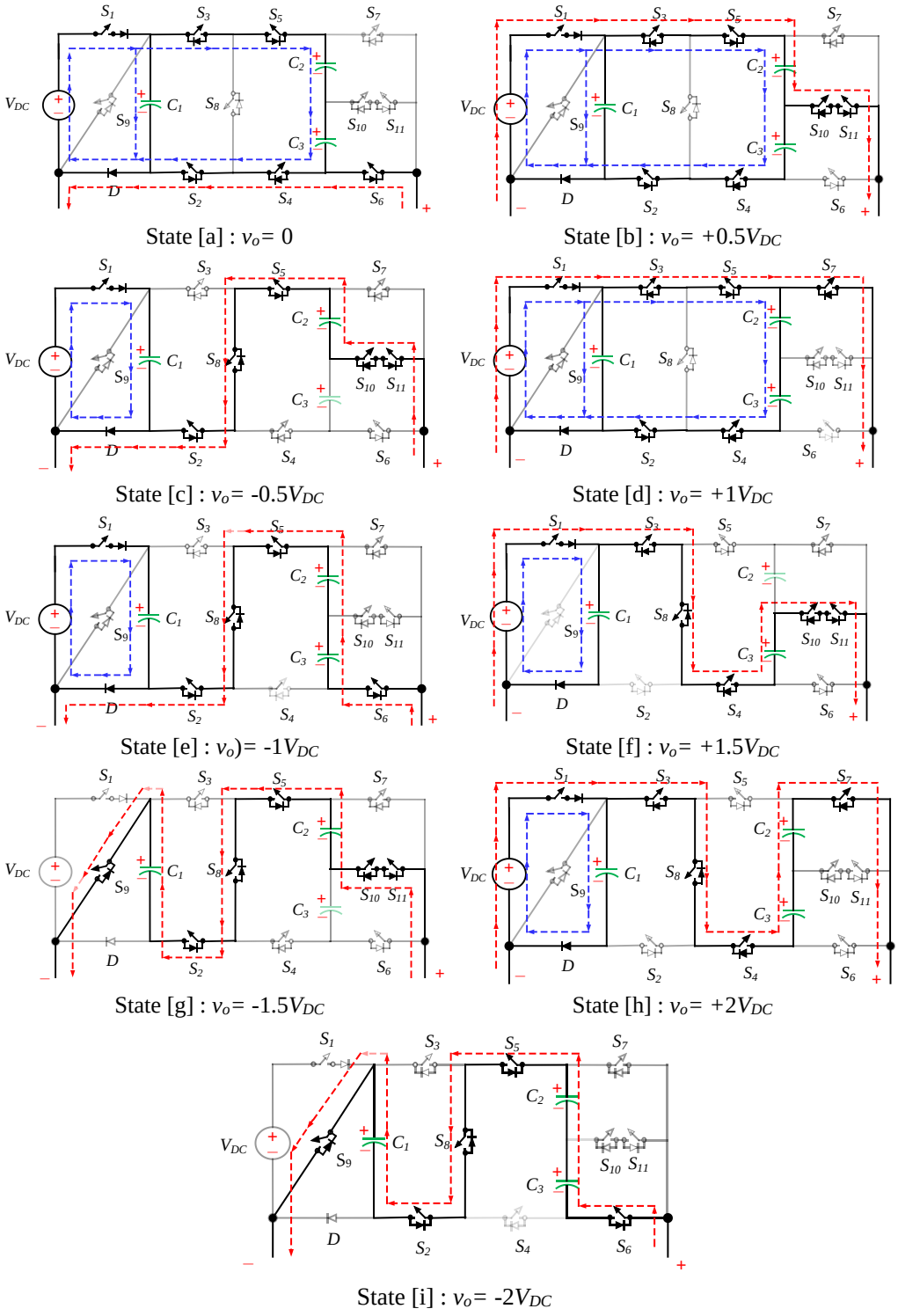



Fig. 3. Equivalent circuits for different switching states of the proposed topology; [a]: $v_0 = 0$, [b]: $v_0 = +0.5V_{DC}$, [c]: $v_0 = -0.5V_{DC}$, [d]: $v_0 = +1V_{DC}$, [e]: $v_0 = -1V_{DC}$, [f]: $v_0 = +1.5V_{DC}$, [g]: $v_0 = -1.5V_{DC}$, [h]: $v_0 = +2V_{DC}$, [i]: $v_0 = -2V_{DC}$

### 2.2. Operational modes

Fig. 3 illustrates the operational analysis of the synthesized output voltage level during capacitor charging and discharging. It has been observed from the switching states that capacitor $C_1$ charged to the input voltage ($V_{C1} = V_{DC}$) during all the states except state (G) and state ($I$). The capacitors $C_2$, $C_3$ are equally charged to half of the input voltage ($V_{C2} = V_{C3} = \frac{1}{2}V_{DC}$) during the state (A), state (B), and state (D). These charging features ensured that the voltages of the three capacitors would remain in balance. The switches $S_1$, $S_2$, $S_3$, $S_4$, $S_5$, $S_6$ are activated for zero levels i.e. $v_0 = 0$. First and second positive voltage levels ($+0.5V_{DC}, +1V_{DC}$) is produced by the input source. The

Table 2. Different modulation index and resulting output level.

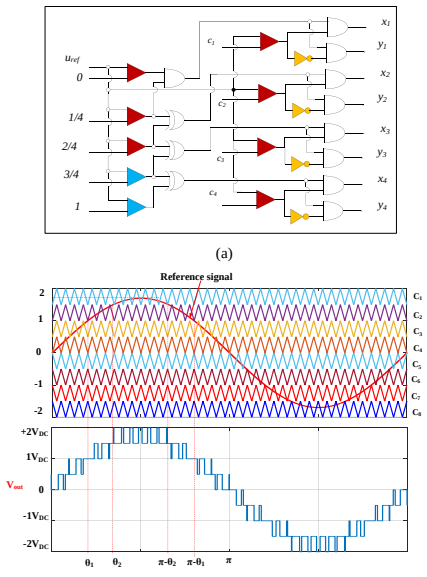
| Modulation index(M) | Output level |
|---|---|
| $0 < M < 1/4$ | 3 |
| $1/4 < M < 2/4$ | 5 |
| $2/4 < M < 3/4$ | 7 |
| $3/4 < M < 1$ | 9 |

negative voltage level ($-0.5V_{DC}$) is produced by $C_2$ and voltage level ($-1V_{DC}$) by $C_2$, $C_3$. Afterward, $C_2$ release their stored energies along with ($V_{DC}$) to the load to produce $+1.5V_{DC}$ and negative voltage level $-1.5V_{DC}$ produced by $C_1$, $C_2$. Similarly, a voltage level $+2V_{DC}$ produced by $C_2$, $C_3$, along with the input source $V_{DC}$ and $-2V_{DC}$ by $C_1$, $C_2$, and $C_3$.

### 2.3. Self-voltage balancing mechanism and design technique of capacitor

As shown in Fig. 2, the capacitor $C_1$ is charged during the level of $\pm1$, and 0 to $V_{DC}$, and $C_2$ charged to $2V_{DC}$ during the voltage level of $\pm2V_{DC}$. The capacitor $C_1$ and $C_2$ discharges their stored energy during the level of voltage $\pm2V_{DC}$ and $\pm3V_{DC}$ respectively. The continuous process of charging/discharging over one fundamental cycle of voltage makes the capacitor self-balanced automatically irrespective of load [6].

Capacitors in SCMLIs serve a crucial function in the transmission and conversion of electrical power. Their voltage fluctuations should be kept under control. The capacitance, load value, and discharging times of capacitors are all interconnected and contribute to the voltage ripple they produce. The output voltage quality, ripple losses, and inverter efficiency can all benefit from lower voltage ripple. The proposed seven-level inverter utilizes two capacitors with identical capacitance. Two capacitors were chosen using the same criteria. Therefore, voltage ripples of the capacitor play a substantial role in the SC inverter design. These ripples should be maintained within a permissible limit. Moreover, voltage ripples are related to the load value, capacitance, and maximum discharging period of the capacitors. The longest discharge times for capacitors $C_1$ and $C_2$ are depicted in Fig. 4-(b) as $(\theta_1,\ \pi-\theta_1)\,(\theta_2,\ \pi-\theta_2)$ respectively. Hence, the discharge amount of the capacitor $C_1$, $C_2$ is calculated as:




(a)

(b)

Fig. 4. (a) Diagrammatic representation of the modulation scheme (b) Reference, carrier and load voltage.

Table 3. Comparative analysis with the recent sc transformerless topologies.

| [Ref.] | $N_L$ | $N_S$ | $N_{SW}$ | $N_C$ | $N_d$ | $F_{C/L}$ | Gain |
|---|---|---|---|---|---|---|---|
| [5] | 5 | 1 | 7 | 3 | 2 | 2.6 | 1 |
| [6] | 4 | 1 | 4 | 4 | 2 | 2.75 | 1.5 |
| [7] | 5 | 1 | 6 | 3 | - | 2 | 0.5 |
| [10] | 5 | 1 | 8 | 4 | 6 | 3.8 | 0.5 |
| [11] | 3 | 1 | 5 | 2 | - | 2.6 | 1 |
| [12] | 5 | 1 | 6 | 3 | 1 | 2.4 | 1 |
| [13] | 3 | 1 | 5 | 2 | - | 2.66 | 1 |
| [14] | 3 | 1 | 4 | 2 | 1 | 2.66 | 1 |
| [15] | 5 | 1 | 8 | 3 | - | 2.4 | 1 |
| [p] | 9 | 1 | 11 | 3 | 1 | 1.66 | 2 |

Where, $N_{dri}$, $N_{sw}$ and $N_s$ are number of drivers, switches, and sources respectively.

Table 4. Comparison with recent MLI configuration.

| Ref. | $N_L$ | $N_S$ | $N_{SW}$ | $N_C$ | $N_D$ | $N_{Dri}$ | $MBV$ | Gain | $F_{C/L}$ |
|---|---|---|---|---|---|---|---|---|---|
| [20] | 5 | 1 | 6 | 1 | 1 | 6 | 2 | 2 | 3 |
| [21] | 9 | 1 | 12 | 4 | - | 12 | 1 | 1 | 3.22 |
| [22] | 9 | 1 | 11 | 2 | - | 11 | 2 | 2 | 2.8 |
| [23] | 9 | 1 | 11 | 3 | - | 11 | 1 | 2 | 2.9 |
| [24] | 5 | 1 | 10 | 2 | - | 10 | 1 | 1 | 4.4 |
| [p] | 9 | 1 | 11 | 3 | 1 | 11 | 1 | 2 | 1.66 |

$$\Delta Q_i = \int_{\theta_x}^{\theta_y} I_{max} \sin(\omega\theta - \emptyset)\, d\theta \tag{5}$$

$$\Delta Q_i = C * \Delta V_{Ci} \tag{6}$$

$$\Delta V_{C1} = \frac{1}{\omega C1} \int_{\theta_1}^{\pi-\theta_1} \frac{1.5V_{DC}}{R} d\theta \tag{7}$$

$$\Delta V_{C1} = \frac{1.5V_{DC}}{\omega R C_1} [\pi - 2\theta_1] \tag{8}$$

$$\Delta V_{C2} = \frac{1}{\omega C2} \int_{\theta_2}^{\pi-\theta_2} \frac{2V_{DC}}{R} d\theta \tag{9}$$

$$\Delta V_{C2} = \frac{2V_{DC}}{\omega R C_2} [\pi - 2\theta_2] \tag{10}$$

$$\Delta V_{C3} = \frac{1}{\omega C3}\left[\int_{\theta_1}^{\pi-\theta_1} \frac{1.5V_{DC}}{R} d\theta + \int_{\theta_2}^{\pi-\theta_2} \frac{2V_{DC}}{R} d\theta\right] \tag{11}$$

$$\Delta V_{C3} = \frac{V_{DC}}{\omega R C_3} [3.5\pi - 4\theta_2 - 3\theta_1] \tag{12}$$

$$\theta_1 = \sin^{-1}\left(\frac{\frac{1}{2}M}{2\pi f}\right) \tag{13}$$

$$\theta_2 = \sin^{-1}\left(\frac{\frac{1.5}{2}M}{2\pi f}\right) \tag{14}$$

The optimal values for capacitance can be stated as follows:

$$C_{\text{optimum,i}} > \frac{\Delta Q_{Ci}}{\Delta V_{Ci}} \tag{15}$$

Table 5. Simulation and experimental parameters.

| Circuit parameter | Specification |
|---|---|
| Input DC source (VDC) | 50V |
| Fundamental frequency ($f_0$) | 50Hz |
| Carrier frequency | 2KHz |
| Impedance | R=35Ω, L=80mH |
| R-load | R=35Ω |
| Capacitors ($C_2$=$C_3$) | 11000$\mu$ F |
| Capacitors ($C_1$) | 2200$\mu$ F |
| Power switches (IGBTs) | GW30NC120HD |
| dSPACE DS 1104 | - |
| Modulation index (M) | 0.95 |

Table 6. Parameters for experimental setup in grid-connected mode.

| Parameters | Value |
|---|---|
| Power rating | 0.5kW |
| Filtering component inductance | 3mH |
| RMS voltage | 250V |
| Grid frequency | 50Hz |
| Switching frequency | 2kHz |
| Filter inductance winding resistance | 0.1Ω |

## 3. SWITCHING AND CONTROL STRATEGY

There are mainly three forms of pulse width modulation (PWM), carrier wave PWM, selective harmonic elimination PWM (SHE-PWM), and space-vector PWM. Since the switching frequency can be reduced using SHE-PWM, switching losses can be reduced and DC voltage can be used more efficiently. However, this is difficult to put into practice. SV-PWM technology can be used by inverters with three to five voltage levels. However, due to its complexity, it is unsuitable for inverters that produce more than five voltage levels.

In this study, we employ a specific type of carrier wave PWM known as phase disposition PWM (PD-PWM) to generate the switching signals. This method simplifies the control circuit due to its straightforward construction. To generate pulses for a nine-level inverter, eight triangular carriers and a sinusoidal modulation wave are required. Each switch's on and off states are determined by a unique logic combination of these pulses. Fig. 4-(a) illustrates modulation for only the positive half of the cycle, with a similar approach applied to the negative half. Each of the eight triangular carriers is transmitted at a constant amplitude (Ac) and carrier frequency (fc) but with distinct phase shifts. The sinusoidal modulation wave is characterized by the output frequency (fo) and reference amplitude (Aref). The modulation index is determined by the amplitudes of the carrier and reference waveforms, defining the modulation index (M).

$$M = \frac{A_{ref}}{3A_c} \tag{16}$$

The suggested inverter can adopt its output to match any changes in "M ". Table 2 shows the different modulation index and the resulting output level.

## 4. LOSSES ANALYSIS

The efficiency of the proposed arrangement can be determined by evaluating the given statement:

$$\eta = \frac{\text{output}}{\text{output} + \text{total losses}} \times 100 \tag{17}$$

The total losses of the proposed configuration encompass the cumulative impact of both switching losses and conduction losses.

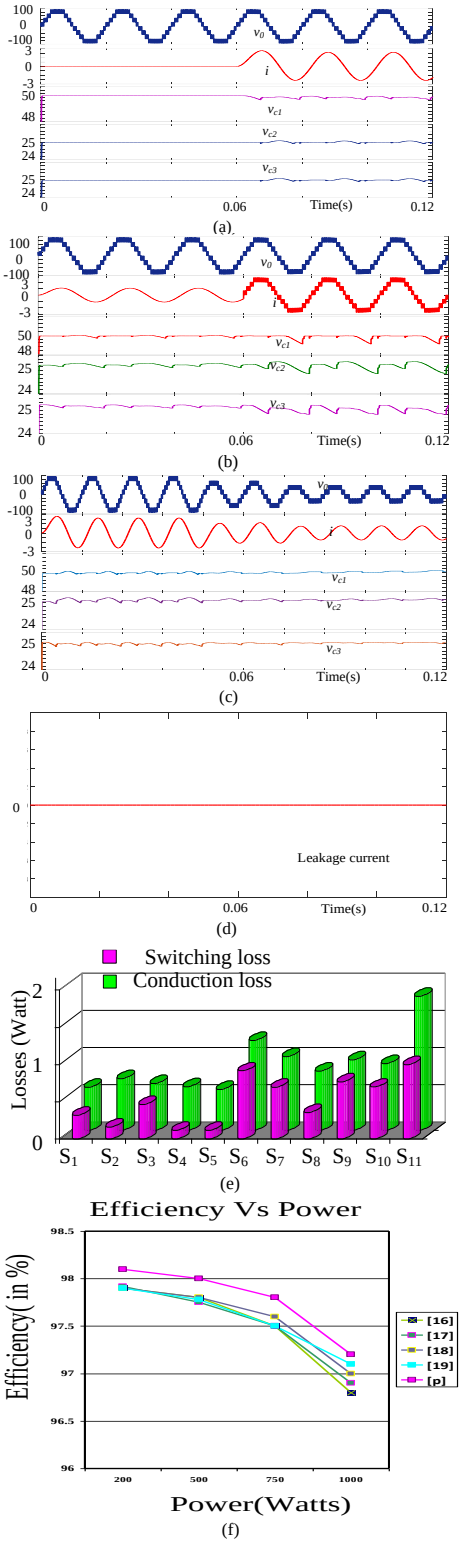



Fig. 5. Simulation results, showcasing (a) No load to steady condition, (b) A step change in load, (c) Variations in supply voltage, (d) Leakage current (e) Loss analysis (f) Efficieny comparision.

### 4.1. Switching losses

Switching losses occur during the transition from the on to off or off to on position. The power dissipated due to the act of turning on and off the $i^{th}$ power switch can be mathematically expressed as:

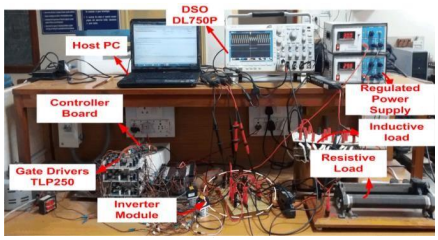



Fig. 6. Main parts of the experimental setup.

$$P_{sw,\ on,\ i} = \frac{1}{6} f\left(VI_{on,\ i} t_{on,i}\right) \tag{18}$$

$$P_{sw,off,i} = \frac{1}{6} f\left(VI_{off,i} t_{off,\ i}\right) \tag{19}$$

Hence, the total power losses attributed to switching ($P_{sw}$) in the proposed configuration can be formulated as:

$$P_{sw} = \sum_{i=1}^{12} \left( \sum_{m=1}^{n_{on,\ i}} P_{sw,\ on,\ im} + \sum_{m=1}^{n_{off,\ i}} P_{sw,\ off,\ im} \right) \tag{20}$$

$n_{on,i}$, and $n_{off,i}$: $i^{th}$ power switch being turned on and off, in a single cycle

V: Blocking state voltage

$I_{on}$, $I_{off}$: currents that occur right after and right before the power switch is turned on

### 4.2. Conduction losses

Conductive losses manifest when switching components are in an active state at varying voltage levels. Therefore, the power dissipation associated with the switches and diodes in the suggested configuration can be expressed as:

$$P_{Con,\ sw,\ i=} \sum_{l=1}^{9} \left( \sum_{i=1}^{n} \left( V_{on,\ sw,\ i} i_{avg,\ sw,\ i} + R_{on,\ sw,\ i} i^2_{rms,\ sw,\ i} \right) \right) \tag{21}$$

$$P_{Con,\ d,\ i=} \sum_{l=1}^{9} \left( \sum_{i=1}^{n} \left( V_{on,\ d,\ i} i_{avg,\ d,\ i} + R_{on,\ d,\ i} i^2_{rms,\ d,\ i} \right) \right) \tag{22}$$

$V_{on,sw,i}$, $V_{on,d,i}$: on-state voltage of $i^{th}$ switch and diode

$i_{avg,sw,i}$, $i_{avg,d,i}$: average on-state current of $i^{th}$ switch and diode

$i_{rms,sw}$, $i_{rms,d}$: RMS current through the switch and diode

$R_{on\ sw,i}$, $R_{on\ d,i}$: internal resistance for $i^{th}$ switch and diode

## 5. COMPARATIVE STUDY

This is important to proving the correctness and utility of the suggested topology. As can be seen in Table 3, two of the most crucial features when comparing to existing state-of-the-art topologies are the number of components per level and the voltage gain. Component per level ($F_{C/L}$) is a factor that may be described as:

$$F_{C/L} = \frac{N_{sw} + N_d + N_c + N_{dri}}{N_l} \tag{23}$$

The cost, weight, and size of the inverter are determined by this $F_{c/l}$ factor. The number of switches is crucial since they are linked to the system's driving unit, heat sink, and protective unit, all of which increase the system's overall mass, dimensions, and costs. Table 3 shows that without the ability to raise voltage, topologies [7], [10] provide five levels. i.e. half again the voltage input. More switching components are used in topology [15] to reduce LC. In order to generate their unique voltage levels, topologies [5, 6], [11], [13], and [14] use a greater number of active and passive components. None of these alternate topologies, however, offers as many benefits as the one that was offered. In comparison to the topologies recommended in [14], [12], which have more active elements per level, these topologies have fewer passive elements overall and no boosting potential.

Results from [20, 22–24] for the same voltage gain demonstrate that the proposed methodology provides a unity voltage stress across the switching components and a lower part count per level. Furthermore, Table 4 demonstrates that the proposed topology is superior to the recently proposed topologies.

## 6. RESULTS AND DISCUSSION

### 6.1. Simulation results

A simulation model was created to assess the viability of the proposed 9-level transformer-less topology. Table 5 furnishes details of the simulation parameters.

The simulation results are illustrated in Figs. 5(a-d). Fig. 5-(a) displays the outcomes under no-load and steady-state conditions. The figure demonstrates that the proposed architecture yields nine levels, reaching up to 100V, with uniform stepping. Fig. 5-(b) reveals that even under sudden changes in loading, the peak values of the load voltage remain intact. In addition, the capacitor's ability to balance itself has been maintained. Fig. 5-(c) illustrates decrase in the supply voltage from 50V to 25V. Fig. 5-(d) depicts the proposed topology's leakage current. Leakage current is shown to be completely eliminated as a result of the proposed design.The proposed topology can easily adapt to new circumstances and yet function adequately. Fig. 5-(e) displays the loss analysis of the proposed topology. Furthermore, a comparison of efficiency has been conducted in Fig. 5-(f), demonstrating that the suggested approach exhibits superior efficiency during load changes.

### 6.2. Experimental validation

Table 5 provides a summary of the laboratory prototype's specifications. To ensure the viability of the recommended MGSCIT, it has been validated under steady-state and transient conditions by a laboratory prototype. A photograph of the experimental setup is shown in Fig. 6.

Figs. 7(a-d) displays the experimental results for both states. Steady-state performance is depicted in Fig. 7-(a). According to observations, the proposed MGSCIT produces a 7-level output with a peak voltage of 150Vand both the capacitors are self-balanced with small voltage ripples. Capacitor $C_1$ and $C_2$ voltage is balanced on 50V and 100 V without the use of sensors or any other supplementary techniques. Transient conditions results such as sudden load change, switching frequency, and magnitude of modulation index (M) are shown in Figs. 7(b-d). The experimental resultfor the sudden shift in load circumstance has been presented in Fig. 7-(b). Voltage level has been confirmed to be constant at its maximum value of 150V. In response to this variation in load, the capacitors' discharging current is affected, and the capacitors' voltage ipplees decrease in value. The change in magnitude of M is shown in Fig. 7-(c). It has been observed that it generates 7-level, 5-level, and 3-level for the M of 0.95, 0.5, and 0.2 respectively. The change of switching frequency (200Hz-5 kHz) is properly adapted by the proposed MGSCIT which is shown in Fig. 7-(d). It is also observed from the waveform that the inverterquickly changes its transient response in both switching frequencies. Consequently, the proposed topology can make use of the natural balance across a wide range of output values. Rapid convergence during transient processes indicates the proposed inverter's high

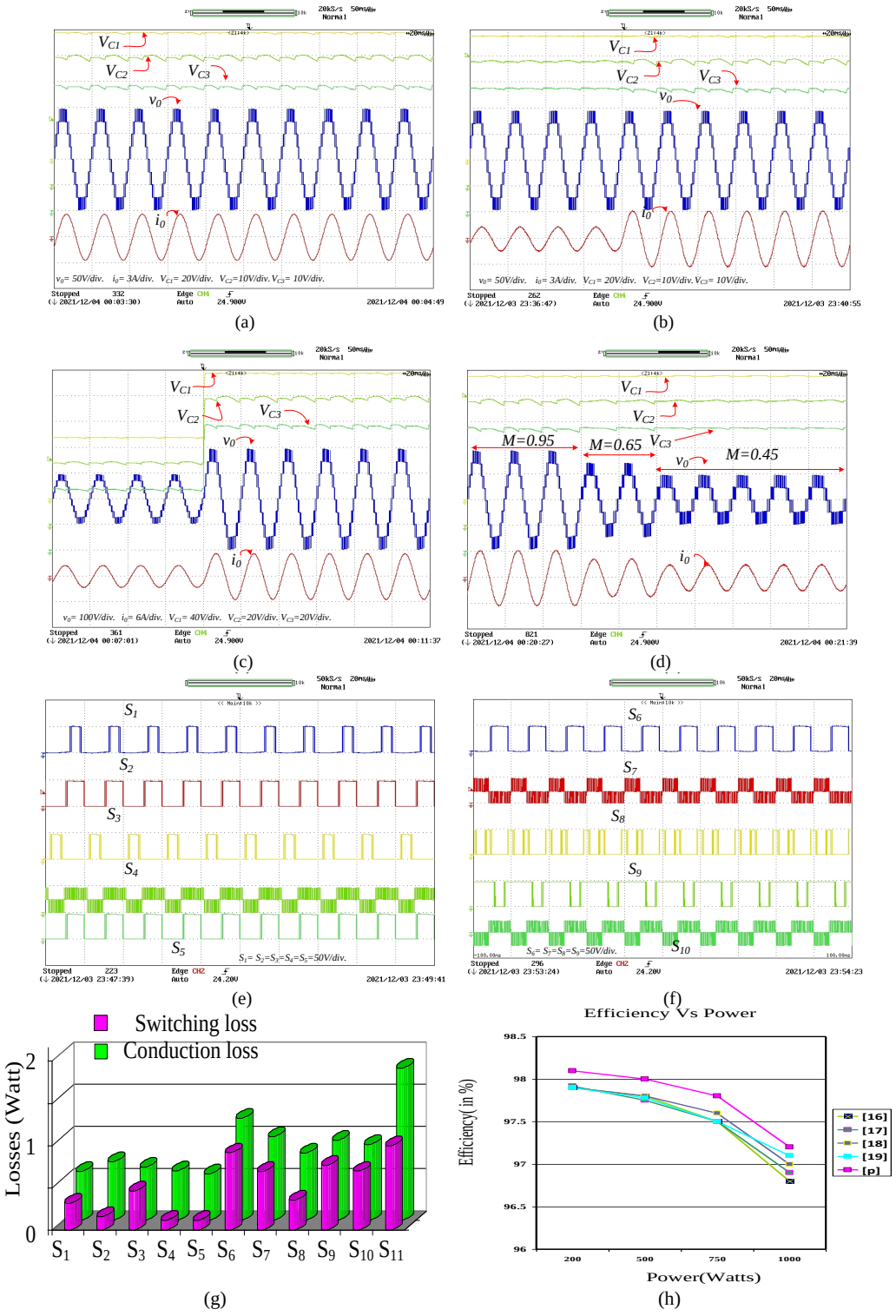



Fig. 7. Experimental result waveform (a) The steady-state condition, (b) A step change in load, (c) Variations in supply voltage, (d) Modulation index transitions, (e) Voltage stress across switch ($S_1$, $S_2$, $S_3$, $S_4$, $S_5$), (f) Voltage stress across switch ($S_6$, $S_7$, $S_8$, $S_9$, $S_{10}$) (g) Loss analysis (h) Efficiency comparison.

dynamic performance. Figs. 7(e-f) shows the voltage stress across the switching componets. In addition to that, an analysis of an efficiency has been incorporated i.e. maximum measured efficiency reaching 96.95%. Figs. 7(g-h) depicts the efficiency in terms of the output power. The topology that has been proposed offers the highest efficiency, which can reach 500W. The overall experimental results show a good steady-state and transient performance of the proposed MGSCIT.

### 6.3. Grid-connected mode:

When linked to the grid, the primary aim of the control strategy is to generate a sinusoidal current aligned with the

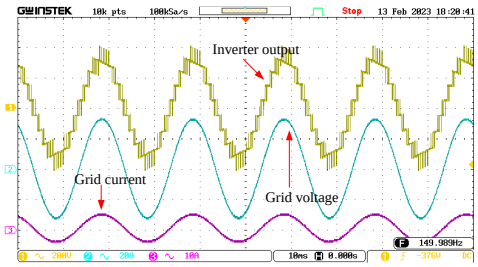



Fig. 8. Experimental result with grid connection.

grid voltage while keeping harmonic distortion to a minimum. The suggested single-phase inverter employs a PR controller to accurately follow the sinusoidal reference current and achieve high gain at a designated frequency. In the subsequent section, the transfer function of the PID controller is elucidated.

$$G_{PR}(s) = K_p + \frac{2K_r\omega_c s}{S^2 + 2\omega_c s + \omega_0^2} \tag{24}$$

The values of $k_P$, $k_r\omega_c$ represent the proportional gain, infinite gain, and resonant frequency. To assess the feasibility of using the proportional-resonant (PR) controller for grid-connected operations, the suggested design underwent testing in a model setup. Table 6 presents the parameters utilized in the experimental configuration. Fig. 8 visually represents the results of the experiment with grid connection. The inverter's output voltage displays a waveform with nine discernible levels, peaking at 400V. Experimental findings clearly indicate perfect phase synchronization between the proposed switched-capacitor (SC) inverter delivering 0.5 kW of real power and the grid's voltage and current. This synchronization provides a solid basis for asserting the capability of the proposed inverter to achieve unity power factor operation. The investigation conclusively establishes that the suggested inverter operates perfectly and without a glitch when connected to the grid.

## 7. CONCLUSION

This research proposes a topology for a transformerless, single-phase SC inverter. The proposed architecture has the advantages of avoiding LC, reducing voltage stress, and utilizing fewer switching components and self-regulating capacitors. The proposed architecture is better suited for a grid-tied renewable energy system because of its capacity to improve the voltage. To illustrate the effectiveness of the suggested topology in comparison with other similar topologies, a comparison table was developed. The results of the simulations are consistent with one another and demonstrate the novelty of the proposed conception. Furthermore, the proposed topology boasts an impressive efficiency rating of 96.9%. Finally, a prototype has been created in the study to verify the theoretical survey's accuracy.

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