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Research Paper

Modelling and Control of a High-Step-Up Enhanced Super-Lift Converter

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Abstract— *Step-up DC-DC converters are essential components used in a wide range of applications. Many researchers have proposed various methods to achieve high voltage gain in DC-DC converters. However, this typically involves adding multiple passive components, which increases system complexity and complicates output voltage control. Maintaining a constant output voltage at the desired value is critical in these converters despite the load, supply voltage changes, and circuit disturbance. Recently, a snubber-less high-step-up enhanced super-lift converter has been developed as a possible solution to these issues. This converter offers high gain without high voltage stress or snubber losses. A model of the converter was created using the state-space averaging technique and is presented in this paper. The control strategy proposed uses the input current in the inner loop and the output voltage in the outer loop. The paper also includes simulation and experimental results that validate the circuit analysis equations.*

Keywords—High-gain DC-DC converter, voltage lift technique, coupled inductor, state space average modelling, cascade control.

1. Introduction

DC-DC converters are now an essential part of many applications, such as voltage regulators, hybrid vehicles, power factor correction, uninterrupted power supplies, motors, spacecraft, and renewable energy systems. Renewable energy sources typically produce direct current (DC) voltage, while most consumer devices require alternating current (AC) voltage. Therefore, it is crucial to convert the output voltage of renewable energy sources into AC voltage using an inverter. To supply DC link inverters, typically 230V and 400V voltages are required for single-phase and three-phase systems, respectively [1–3]. To generate high voltage levels from renewable energy sources, multiple solar panels need to be connected in series. However, this approach can result in various challenges such as increased ground occupancy, reduced controllability, and shadow effects. To address these issues, Step-Up DC-DC converters have been developed [4–15]. Various techniques have been developed for Step-Up DC-DC converters. One of these techniques involves using a multiplier cell (MC) at the output of the DC-DC converter [5]. Another way to achieve high voltage gain is by using a switched inductor/switched capacitors converter or a hybrid combination of both. However, these converters have some disadvantages, such as increased cost and complex control due to the use of multiple components [6], [7]. To increase voltage levels, voltage lift is a common method used that can be implemented in a single-level or multi-level manner [8–10]. Another effective technique is using coupled inductors in combination with any of the aforementioned methods. Although the leakage inductance in the coupled inductance causes spikes across the semiconductor devices, it increases the converter losses. These converters can increase voltage gain efficiently if voltage spikes are limited on their semiconductor devices [11]. One of the ways to reduce spike voltage is to use active clamps and passive clamps in converters. Converter [12] has used a lossless method to recover the energy of the leakage inductor. However, the limited voltage gain necessitated the use of an interleaving method in the input and series output to increase voltage gain. By using the interleave method, the number of components in [13] has been doubled compared to [12].

[16] provides a detailed description of the modeling and control of the boost converter with the voltage multiplier cell. Specifically, for a duty cycle of 76%, the voltage gain value is 8.3. In addition, reference [17] details the modeling of a high-voltage DC-DC converter and the use of coupling inductors. For a duty cycle of 60%, the voltage gain is 12.

In this paper, the control approach of a high-step-up DC-DC converter based on self-coupling and super lift techniques [18] is presented. The high-gain DC-DC converter, referred to as converter [18], is based on the super-lift topology and coupled inductor structure. This converter recovers energy stored in the leakage inductance of the coupled inductor back to the circuit. As a result, it offers an ultra-gain without inducing high spike voltage on the semiconductor devices and snubber losses. We model the converter and subsequently design a control system to regulate the output voltage at the desired value. The circuit diagram of this converter is illustrated in Fig. 1.

The structure of the paper is organized as follows: in section 2 demonstrates the analysis of the converter's performance in CCM. in section 3 presents voltage gain and voltage stress on the semiconductor devices. Dynamic behavior is illustrated in section

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4. in section 5 focuses on the modeling design of passive elements. The design of the compensator for controlling both voltage and current modes in the proposed converter is presented in section 6. Finally, in section 7 presents the simulation and experimental results obtained.

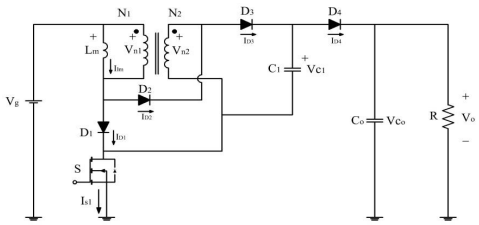


Fig. 1. High step-up DC-DC converter based on a coupled inductor and super lift topology [18].

2. OPERATION PRINCIPLE

The high-step-up enhanced super-lift converter, as shown in Fig. 1, consists of several components, including the main switch S, three diodes (D_1, D_2, and D_3), two capacitors (C_1 and C_2), and a coupled inductor. The magnetizing inductance of the coupled inductor is represented by the symbol L_m, while N_1 and N_2 refer to the number of turns in the primary and secondary windings of the coupled inductor. In order to derive the dynamic model of the high-step-up enhanced super-lift converter, we make the assumption that:

- All components are functioning optimally, and the converter is operating in a stable condition.
- The inductors and capacitors are assumed to be large enough, and their corresponding currents and voltages are considered during a fixed switching period.
- The losses associated with semiconductors are not taken into consideration.

This converter has three operation stages in continuous current mode (CCM). Fig. 2 depicts equivalent circuits during three modes, and Fig. 3 shows the waveform of the circuit elements.

2.1. Mode 1 [t_0-t_1]

During this time interval, the active switch is turned on. The diodes D_1 and D_3 are forward-biased Also, the magnetizing inductor current i_{Lm} increases linearly. Capacitor C_1 starts charging through diode D_3. This mode ends when current of the diode D_1 is equal to the magnetizing inductor current. The flow path of this mode is shown in Fig. 2-(a). The governing equations of the converter are as follows:

$$\dot{i}_{Lm} = i\frac{v_{C1}}{L_m N_{21}} \tag{1}$$

Where V_{C1} is the voltage of the capacitor C_1, and N_{21} is the urn ratio of the coupled inductor ($N_{21} = N_2/N_1$). Using the KCL for the capacitors C_1, it can be written that:

$$\dot{v}_{C1} = (i_g - i_{Lm})\frac{1}{C_1 N_{21}} \tag{2}$$

Where i_g is the input current and is defined as:

$$i_g = \frac{V_g - L_m \dot{i}_{Lm}}{R_i} \tag{3}$$

Given Eqs. (1) and (3) into Eq. (2):

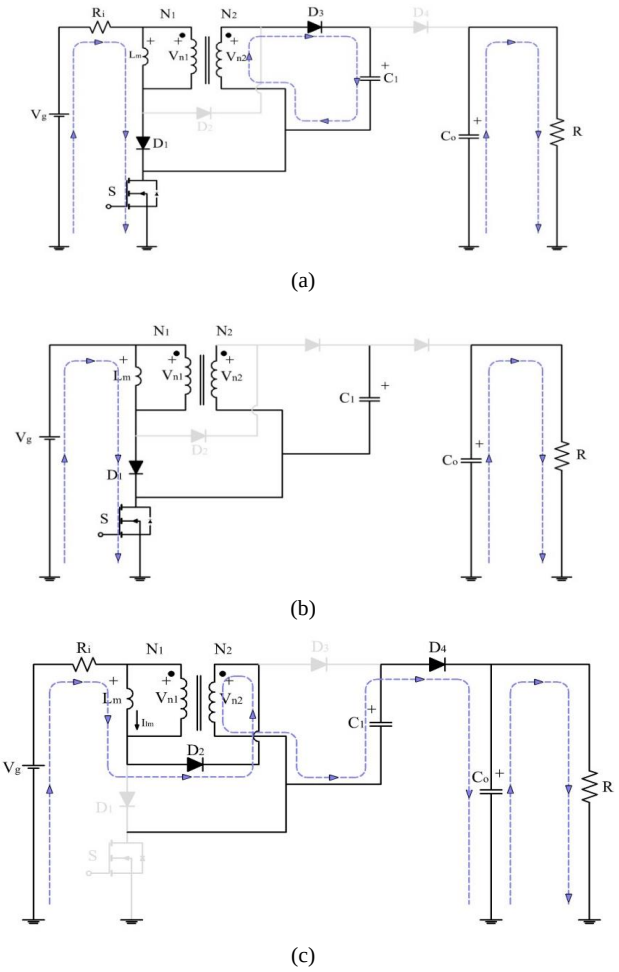


Fig. 2. Operation mode of the converter. (a) Mode 1. (b) Mode 2. (c) Mode 3.

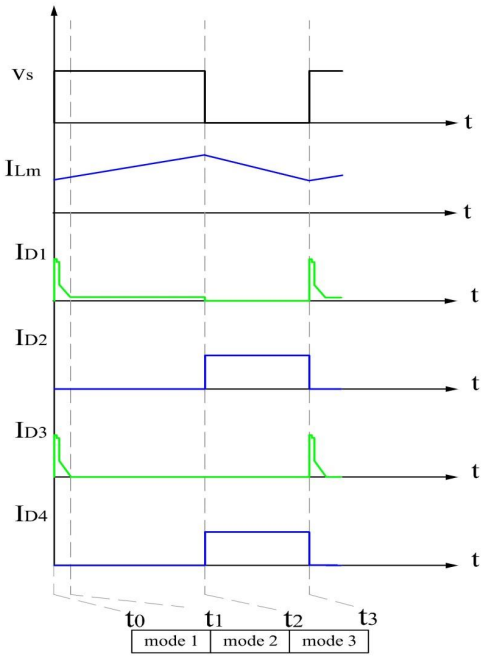


Fig. 3. Characteristic waveform of the converter in CCM.

$$\dot{v}_{C1} = \left(\frac{V_g - \frac{v_{C1}}{N_{21}}}{R_i} - i_{Lm} \right) \frac{1}{C_1 N_{21}} \tag{4}$$

For the output capacitance of C_o, it can be expressed that:

$$\dot{v}_{CO} = \frac{v_{CO}}{C_O R} \tag{5}$$

Equations above can be represented as state space matrices:

$$\begin{cases} \dot{x}(t) = A_1 x(t) + B_1 V_g \\ y(t) = C_1 x(t) + E_1 V_g \end{cases} \tag{6}$$

where $x(t) = \begin{bmatrix} i_{Lm} & v_{c1} & v_{co} \end{bmatrix}^T$ and $y(t) = [i_g]$. The matrix values A_1, B_1, C_1, and E_1 can be written as follow:

$$A_1 = \begin{bmatrix} 0 & \frac{1}{L_m N_{21}} & 0 \\ -\frac{1}{N_{21}} & -\frac{1}{{N_{21}}^2 R_i} & 0 \\ 0 & 0 & -\frac{1}{C_O R} \end{bmatrix} \tag{7}$$

$$B_1 = \begin{bmatrix} 0 & \frac{1}{N_{21} R_i} & 0 \end{bmatrix}^T \tag{8}$$

$$C_1 = \begin{bmatrix} 0 & -\frac{1}{N_{21} R_i} & 0 \end{bmatrix}^T \tag{9}$$

$$E_1 = \frac{1}{R_i} \tag{10}$$

2.2. Mode 2 [t_1-t_2]

At this moment, the Switch is still turned on. The magnetizing inductor is being charged by connecting the switch and diode D_1. Meanwhile, the diodes D_2, D_3, and D_4 are reverse biased and cut off. The output capacitor is also discharging into the load. During this time, you can confirm that the equations for magnetizing inductor and output capacitor are similar to the previous state. Also, capacitor voltage C_1 remains unchanged, and its derivative is zero. You can see the flow path for this mode in Fig. 2-(b).

2.3. Mode 3 [t_2-t_3]

At the beginning of this time interval, the active switch is turned off. The diodes D_2 and D_4 are in forward bias and connected. The magnetic inductor current flows through diode D_2 and into the output. The output capacitor is charged through the magnetic inductor, secondary transformer, and capacitor C_1. This mode ends when the switch is turned off again. The flow path of this mode is shown in Fig. 2-(c). Once this mode is over, the previously described modes will be repeated. In this mode, the voltage of the magnetic inductor can be written as follows:

$$\begin{aligned} &-V_g + L_m \dot{i}_{Lm} + N_{21} L_m \dot{i}_{Lm} - \\ &v_{C1} + v_{CO} + R_i i_g = 0 \end{aligned} \tag{11}$$

From Eq. (11), it can be expressed that:

$$\begin{aligned} &\dot{i}_{Lm} = \\ &\frac{1}{(1+N_{21}) L_m} \left[V_g + v_{C1} - v_{CO} - R_i i_g \right] \end{aligned} \tag{12}$$

where in:

$$i_g = \frac{i_{Lm}}{(1 + N_{21})} \tag{13}$$

By substituting Eq. (13) into Eq. (12), it can be written that:

$$\dot{i}_{Lm} = \frac{1}{(1+N_{21})L_m}\left[V_g + v_{C1} - v_{CO} - R_i\frac{i_{Lm}}{(1+N_{21})}\right] \quad (14)$$

Using the KCL for capacitor C_1 , it can be expressed that:

$$\dot{v}_{C1} = (v_{Lm} - i_g)\frac{1}{C_1 N_{21}} \quad (15)$$

Substituting Eq. (13) in Eq. (15) leads to:

$$\dot{v}_{C1} = v_{Lm}\left(1 - \frac{1}{1+N_{21}}\right)\frac{1}{C_1 N_{21}} \quad (16)$$

For the output capacitor of C_o, it can be written that:

$$\dot{v}_{CO} = \frac{1}{C_O}\left(C_1\dot{v}_{C1} - \frac{v_{CO}}{R}\right) \quad (17)$$

By substituting Eq. (16) into Eq. (17), it can be expressed that:

$$\dot{v}_{CO} = \frac{1}{C_O}\left[\left[i_{Lm} \times \left[\frac{1}{1+N_{21}} - 1\right]\frac{1}{C_1 N_{21}}\right] - \frac{v_{CO}}{R}\right] \quad (18)$$

Equations above can be represented as state space matrices:

$$\begin{cases} \dot{x}(t) = A_2 x(t) + B_2 V_g \\ y(t) = C_2 x(t) + E_2 V_g \end{cases} \quad (19)$$

The matrices A_2, B_2, C_2 and E_2 are equal to:

$$A_2 = \begin{bmatrix} -\frac{R_i}{(1+N_{21})^2} & \frac{1}{1+N_{21}} & \frac{1}{1+N_{21}} \\ \left(\frac{1}{1+N_{21}} - 1\right)\frac{1}{C_1 N_{21}} & 0 & 0 \\ -\left(\frac{1}{1+N_{21}} - 1\right)\frac{1}{C_1 C_O N_{21}} & 0 & -\frac{1}{C_O R} \end{bmatrix} \quad (20)$$

$$B_2 = \begin{bmatrix} \frac{1}{N_{21}+1} & 0 & 0 \end{bmatrix}^T \quad (21)$$

$$C_2 = \begin{bmatrix} \frac{1}{N_{21}+1} & 0 & 0 \end{bmatrix}^T \quad (22)$$

$$E_2 = 0 \quad (23)$$

In the second operating mode, the magnetic inductor current increases at the same rate as the first working mode. Therefore, the output capacitor functions in the same way as in the previous operating mode. Additionally, due to the disconnection of diodes D_3 and D_4, no changes are made to capacitor C_1. As a result, it is only necessary to consider the first and third modes when forming the state space matrix and modeling the converter.

Table 1. Comparison of the proposed converter and other similar topologies.

Converter	Gain	#Core	#Capacitor	#Active switch	#Diode
[18]	$\frac{n+1}{1-d}$	1	2	1	4
[6]	$\frac{nd+n+1}{1-d}$	1	4	1	4
[7]	$\frac{n+1}{1-d}$	1	3	1	3
[11]	$\frac{n+1}{1-d}$	1	2	1	2
[12]	$\frac{2+3n-d-nd}{1-d}$	1	5	1	5
[13]	$1+\frac{1+3n+2dn}{1-d}$	2	8	2	9
[14]	$\frac{2n+2}{1-d}$	2	8	5	8
[20]	$\frac{(n+1)(2-d)}{1-d}$	1	4	1	4

3. VOLTAGE GAINS AND VOLTAGE STRESS ON THE SEMICONDUCTOR DEVICES

According to Eqs. (1) and (11) and using the volt-second balance law, the voltage gain of the converter is as follows. For the active switch S, diode D_1 and diode D_3, stress voltage in mode 3 can be calculated as:

$$V_O = \frac{1+N_{21}}{1-d}V_{in} \quad (24)$$

$$V_S = \frac{1+dN_{21}}{1+N_{21}}V_O \quad (25)$$

$$V_{D1} = \frac{dN_{21}}{1+N_{21}}V_O \quad (26)$$

$$V_{D3} = \frac{N_{21}}{1+N_{21}}V_O \quad (27)$$

For diodes D_2 and D_4, stress voltage in mode 1 can be calculated as:

$$V_{D2} = \frac{(1-d)N_{21}}{1+N_{21}}V_O \quad (28)$$

$$V_{D4} = \frac{1+dN_{21}}{1+N_{21}}V_O \quad (29)$$

In Table 1, you can find a comparison between the proposed converter and other high voltage gain converters that are similar. The table presents various components used in different converters, including gains, power ratings of switches, overall power ratings of diodes, and the used components. To calculate the power rating of a switching device, we multiply voltage stress and current stress. As per the analysis, the voltage stress calculated for some converters such as [11, 19] is higher than their ideal model. Though the number of proposed converters is moderate when compared to other converters, the converter proposed in [11] has fewer components. However, it requires additional components for the snubber circuit. In the converter presented in [11], when the switch is turned off, the stored energy in the leakage inductance causes the switch to experience high voltage stress (output voltage). Therefore, a snubber circuit is necessary to resolve the issue [11]. Although transformers [12], [13] and [14] have large voltage gain, the number of their components is much larger than [18].

4. DYNAMIC BEHAVIOUR MODELING USING THE STATE-SPACE AVERAGING TECHNIQUE

According to [21], it is possible to obtain the average state space model.

$$\begin{cases} \langle \dot{x}(t)\rangle_{T_S} = \left[A_1 d(t) + A_2 \acute{d}(t)\right]\langle \dot{x}(t)\rangle_{T_S} + \\ \qquad \left[B_1 d(t) + B_2 \acute{d}(t)\right]\langle V_g(t)\rangle_{T_S} \\ \langle y(t)\rangle_{T_S} = \left[C_1 d(t) + C_2 \acute{d}(t)\right]\langle x(t)\rangle_{T_S} + \\ \qquad \left[E_1 d(t) + E_2 \acute{d}(t)\right]\langle V_g(t)\rangle_{T_S} \end{cases} \tag{30}$$

where the value of $\langle x(t)\rangle_{T_S}$ is the average value of $x(t)$ over a switching period.

By sting $d(t) = d$ and $\langle V_g(t)\rangle_{T_S}$ and setting all derivatives equal to zero, relations of the converter in the steady state are determined:

$$\begin{cases} X = -A^{-1}B_2 V_g(t) \\ Y = -C^{-1}B_2 V_g(t) \end{cases} \tag{31}$$

Where A, B, C and E are defined by Eqs. (32), (33), (34) and (35), respectively.

$$A = A_1 d + A_2 \acute{d} = \begin{bmatrix} -\frac{R_i}{(1+N_{21})^2} & \frac{d}{N_{21}} + \frac{\acute{d}}{1+N_{21}} & -\frac{\acute{d}}{1+N_{21}} \\ \left(\frac{1}{1+N_{21}} - 1\right)\frac{1}{C_1 N_{21}} & -\frac{d}{R_i {N_{21}}^2} & 0 \\ -\acute{d}\left(\frac{1}{(1+N_{21})N_{21}} - \frac{1}{N_{21}}\right)\frac{1}{C_1 C_O N_{21}} & 0 & -\frac{1}{R} \end{bmatrix} \tag{32}$$

$$B = B_1 d + B_2 \acute{d} = \begin{bmatrix} \frac{\acute{d}}{1+N_{21}} & \frac{d}{R_i N_{21}} & 0 \end{bmatrix}^T \tag{33}$$

$$C = C_1 d + C_2 \acute{d} = \begin{bmatrix} \frac{\acute{d}}{1+N_{21}} & \frac{d}{R_i N_{21}} & 0 \end{bmatrix}^T \tag{34}$$

$$E = E_1 d + E_2 \acute{d} = \frac{d}{R_i} \tag{35}$$

The small signal model of the converter is derived by [21]:

$$\begin{aligned} & K\tfrac{d\hat{x}(t)}{dt} = \\ & A\hat{x}(t) + B\hat{V}_g(t) + \\ & \{(A_1 + A_1)X + (B_1 + B_2)U\}\hat{d}(t) \end{aligned} \tag{36}$$

where superscript '^' denotes small signal term of each variable from Eq. (36) it can be expressed that:

$$\hat{x}(t) = (Sk - A)^{-1} d\hat{g}(t) \tag{37}$$

where $\hat{g}(t) = \left[\hat{v}_g(t) \quad \hat{d}(t)\right]^T$. Now Eq. (37) is a linear Equation from which the converter transfer functions can be obtained using Eqs. (38) and (39):

$$\begin{aligned} G_{id} = \left.\tfrac{\hat{i}(s)}{\hat{d}(s)}\right|_{\hat{v}_g=0} = \\ \frac{163840000\times\begin{pmatrix} 10443286345137363S^2 \\ +3517324149102466736300 0S \\ +72798782156289254928000000 \end{pmatrix}}{\begin{aligned} & 65716525762559028125S^3 \\ & +219120836988708665986659 28S^2 \\ & +22608794164104784225900928000S \\ & +23121840774890316103680000000000 0 \end{aligned}} \end{aligned} \tag{38}$$

$$\begin{aligned} G_{vd} = \left.\tfrac{\hat{v}_{co}(s)}{\hat{d}(s)}\right|_{\hat{v}_g=0} = \\ \frac{-2500\times\begin{pmatrix} 703166825659716009375S^2 \\ +2337045676814373787832199296S \\ -22969040244813087878676480000000 \end{pmatrix}}{\begin{aligned} & 6571652576259028125S^3 \\ & +219120836988708665986659 28S^2 \\ & +22608794164104784225900928000S \\ & +23121840774890316103680000000000 0 \end{aligned}} \end{aligned} \tag{39}$$

5. MODELLING DESIGN OF PASSIVE ELEMENT

Designing the circuit components for the converter is a crucial step that requires careful consideration. The selection of appropriate values for inductors and capacitors is a topic that often sparks controversy in the field of DC-DC converters. One effective approach to determine the values of inductors and capacitors is to analyse their impact on the conversion functions of the circuit [22]. When poles are transferred along an imaginary axis, the natural damping frequency changes, resulting in a shift from weak damping to critical damping response. Fig. 4 demonstrates that increasing the amount of magnetizing inductor can help achieve this. However, as depicted in Fig. 5, altering the value of C has little effect on the RHP zeros. Additionally, it has been observed that increasing the amount of magnetizing inductor can lead to a slower system response.

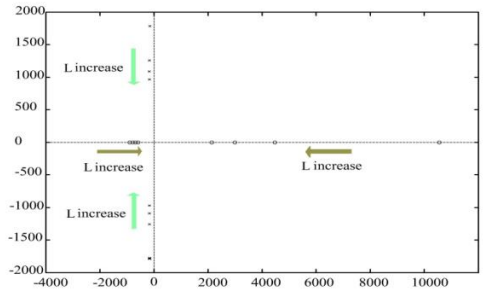


Fig. 4. The effect of capacitor changes on the pole and zero locations.

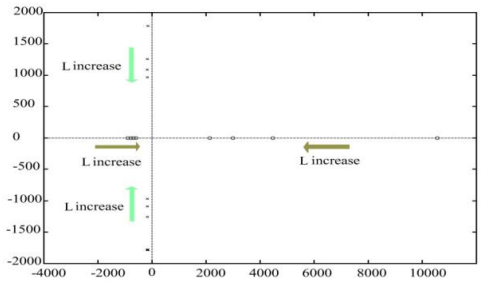


Fig. 5. The effect of magnetizing inductor changes on the location of zero and pole.

6. CONTROLLER

In the previous section, we derived the small-signal model of the converter. In this section, we will introduce a control method for the high step up Enhanced Super-Lift Converter using the parameters listed in Table 2. Fig. 7 illustrates the block diagram of the proposed system, which utilizes voltage and current compensators to regulate the converter. Blocks G_v and G_i represent the input current and output voltage controllers, respectively. H_v which is the output voltage sensor is considered equal to 1 and the pulse

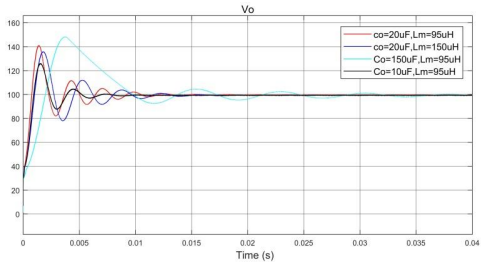


Fig. 6. The step response of the output voltage in exchange for changing the passive values of the converter.

width modulation (PWM) block represents the PWM dynamic model, which can be given by [19–26]. The bode diagram for the transfer functions of control to input current is depicted in Fig. 8. To compensate for voltage variations, a PD compensator can be employed [19–26].

$$G_i(s) = G_{io}\frac{\left(1+\frac{S}{\omega_{iz}}\right)}{\left(1+\frac{S}{\omega_{ip}}\right)} \tag{40}$$

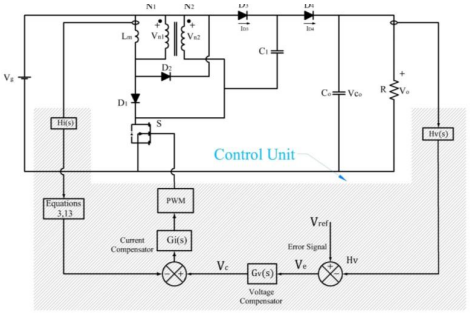


Fig. 7. Block diagram output voltage controller using cascade method.

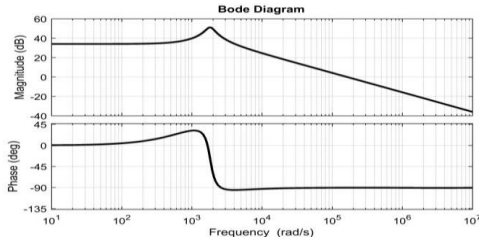


Fig. 8. Bode diagram of G_{id}.

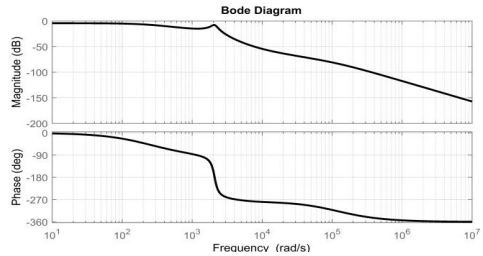


Fig. 9. Bode diagram of open loop transfer function.

For phase margin of 60 degrees and crossover frequency of 5 kHz, the controller can be found as:

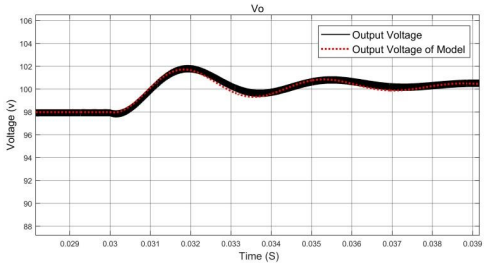
Table 2. Parameters of the converter employed in the modelling.

Parameter	Notation	Value
Input voltage	V_g	8-12V
Output voltage	V_o	80-100V
Rated of output power	P_{out}	16-64W
Switch frequency	f_s	50Khz
Load	R	100-400Ω
Coupled inductor turns ratio	N_{21}	1:3
Magnetizing inductor	L_m	95μH
Capacitor	C_1	10μH
Capacitor	C_o	10μH
diodes	D_1, D_2	V30202C
diodes	D_3, D_4	SBR40U300CT
switch	S	IXFK210N30X3

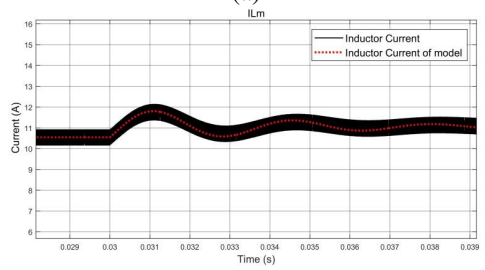
$$G_i(s) = \frac{1.33}{S}\frac{\left(1+\frac{S}{8417.84}\right)}{\left(1+\frac{S}{11724583}\right)} \tag{41}$$

Regarding Fig. 7, closed loop transfer function of current loop can be expressed by:

$$G_{i,CL}(s) = \frac{C_i(S)G_{PWM}(S)G_{id}(S)}{1+C_i(S)G_{PWM}(S)G_{id}(S)H_i(S)H_e(S)} \tag{42}$$



(a)



(b)

Fig. 10. Comparison of transient respond with 1% change in duty cycle in 0.03. (a) Output voltage. (b) Magnetizing inductor current.

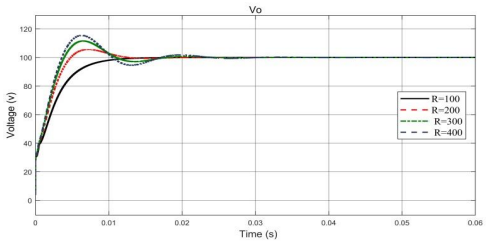
where:

$$G_{PWM}(S) = \frac{1}{3}, \quad H_i(S) = 1/50 \tag{43}$$

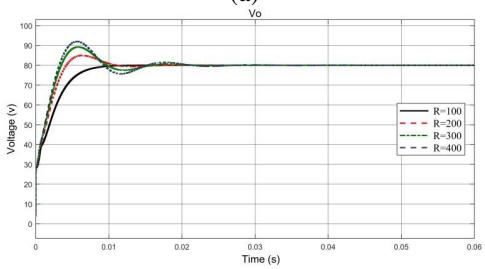
$$H_e(S) = \frac{S^2}{(\pi f_S)^2} - \frac{S}{2f_S} + 1 \tag{44}$$

To design voltage controller, transfer function of output voltage to input current should be extracted:

$$G_{Voi}(S) = \frac{G_{vod}(S)}{G_{ild}(S)} \tag{45}$$

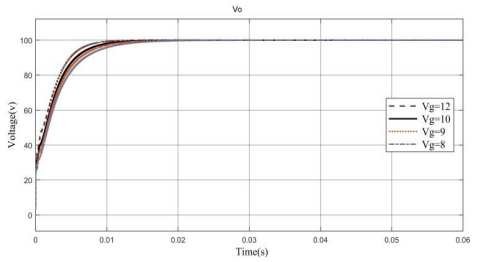


(a)

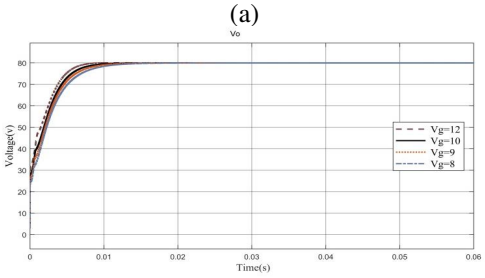


(b)

Fig. 11. (a) Output voltage for reference value100, (b) Output voltage for reference value 80 with 400% change in load.



(a)



(b)

Fig. 12. (a) Output voltage for reference value100, (b) Output voltage for reference value 80, despite 20% change in input voltage.

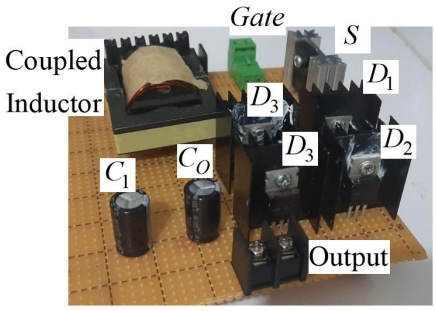


Fig. 13. The view of the experimental prototype of the proposed converter.

Eq. (45) can be calculated using Eqs. (38) and (39). Open loop transfer function of voltage loop can be expressed as:

$$G_{Voi}(S) = G_{icl}(S)\, G_{voil}(S) \tag{46}$$

Fig. 9 shows bode diagram of Eq. (46). To compensate voltage, loop a PD compensate can be used [19–26]:

$$G_v(s) = G_{vo} \frac{\left(1 + \frac{S}{\omega_{vz}}\right)}{\left(1 + \frac{S}{\omega_{vp}}\right)} \tag{47}$$

For phase margin of 50 degrees and crossover frequency of 1/4 f_s Hz, the controller can be found as:

$$G_v(s) = \frac{1.64}{S} \frac{\left(1 + \frac{S}{8417.84}\right)}{\left(1 + \frac{S}{11724583}\right)} \tag{48}$$

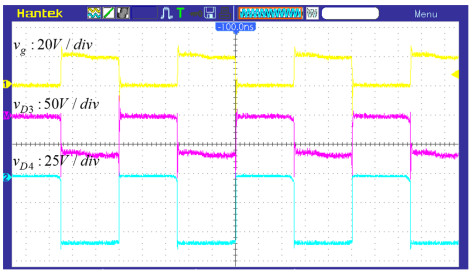


Fig. 14. The voltage across diodes D_3 and D_4.

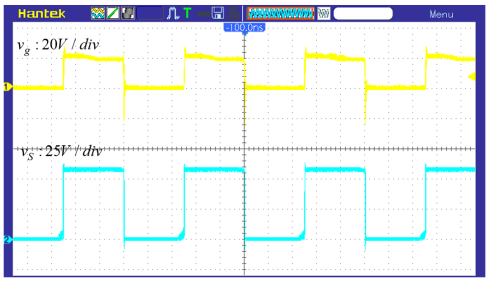


Fig. 15. The voltage across active switch.

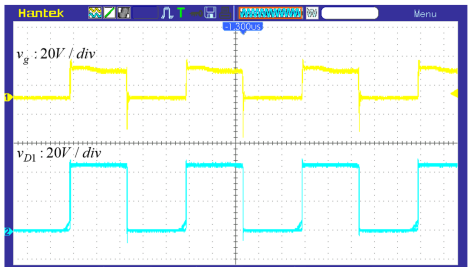


Fig. 16. The voltage across diode D_1.

7. SIMULATION AND EXPERIMENTAL RESULTS

Simulation and experimental results are used to validate the theorical analysis. Table 2 shows the values used to simulate the proposed converter. Fig. 10 shows the results obtained from the simulation and modelling of the proposed converter. As shown in the figure, with a change of 1% in the amount of duty cycle in

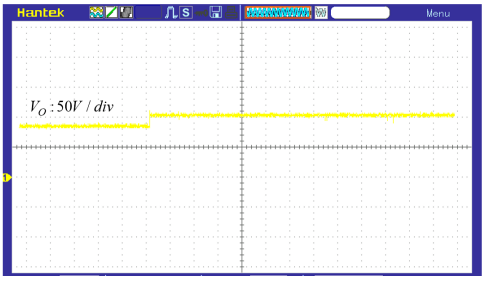


Fig. 17. The step response of proposed converter.

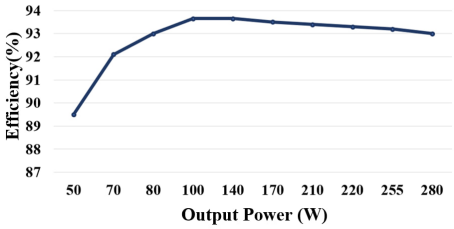


Fig. 18. The efficiency of the proposed converter.

0.03 second, the output voltage waveform and the inductor current resulting from the modelling follow the waveforms resulting from the simulation, which confirms the modelling relations. Fig. 11 shows the value of the converter output voltage by applying the control method presented in the previous section. As shown in the figure, the value of the output voltage under changes of 2,3 and 4 times in the value of load resistance, remains constant at the desired value (Reference values are 100 and 80), which confirms the proposed control method. Fig. 12 shows the output voltage waveform of the proposed converter under changes of 20% in the input voltage, as it is clear that the output voltage value remains constant by applying these changes to the desired value, which confirms the proposed control method.

Fig. 13 depicts the experimental prototype of the proposed converter with Figs. 14-17 showing the experimental waveforms including the switching signal for clarity. In Fig. 14 the voltage of the diodes D_3 and D_4 is displayed. As expected, when the switching signal is high, diodes D_3 and D_4 are off, and according to Fig. 16 the switching signal is synchronized with the turning off and on of the active switch. Also, according to Fig. 16, when the switching signal is high, diodes D_3 and D_4 are on. Furthermore, it is observable that Eqs. (24) to (29) hold true. The dynamic response of the converter by changing the reference value from 80 to 100 V is shown in Fig. 17. Based on the Fig. 18, it can be inferred that the circuit's efficiency falls within the range of 93% to 94%. This makes it an optimal choice for renewable energy applications where high efficiency is a crucial requirement for choosing a converter. The obtained result is evidence of the proposed converter's outstanding performance.

8. CONCLUSION

The objective of this paper was to model and control the voltage and current modes of an amplifier DC-DC converter based on inductance and a super lift structure. The main operating modes of the proposed converter were described in continuous mode. To simplify the modelling of the converter, two primary modes of operation were considered. Additionally, compensating design for the proposed converter was performed based on the conversion functions obtained from modelling the small signal circuit and its diagram. Finally, the voltage and current controllers were successfully implemented on the proposed converter using the derived relationships.

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