

Research Paper

A Low Input Current Ripple High Step-Up DC-DC Converter with Reduced Voltage Stress for Renewable Energy Application

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Abstract—This report develops a high step-up topology employing a voltage multiplier cell (VMC) and a coupled inductor for renewable energy usage. The efficiency is improved and the blocking voltage on semiconductors is decreased. The proposed structure achieves a high voltage gain by utilizing a VMC and one coupled inductor. This structure employs only one MOSFET switch, lowering the cost of the converter. Further benefits are the reduced number of components and the low blocking voltage of the switches/diodes. Furthermore, the VMC functions as a clamp circuit, reducing the peak voltage of the switch. Consequently, in the presented converter, a low nominal voltage MOSFET can be operated. The switching modes, steady-state analysis, and comparative study with other comparable converters demonstrate the converter's performance and superiority. A 200W laboratory scale operating under the 25kHz switching frequency and a voltage conversion of 20V~150V is built to validate the theoretical equations. The proposed converter efficiency at the full load is about 96.3%. Also, the normalized maximum voltage stress on switch and diodes for duty cycle $D=0.6$ and turn ratio $N=2$ is about 0.33 and 0.8, respectively.

Keywords—Renewable energy, power converter, high voltage gain, reduced ripple, low blocking voltage.

1. INTRODUCTION

Renewable energy technologies such as solar, fuel cells (FC), and wind energy are becoming more popular due to the rapid growth in energy dissipation [1, 2]. This issue has prompted power engineering experts, companies, and authorities to broaden their study into renewable energy [3, 4]. The voltage produced by FC and PV is direct current (DC) and has a poor amount. To transform this low voltage to a high value, a high voltage conversion ratio converter is used as an interface unit between the renewable source and the consumer. A high voltage gain, small volume, and lower power loss topology is required for this work. DC-DC converters can boost the voltage value to meet the needs of the load or DC bus [5, 6]. So, to these concerns, the development of high-voltage-gain converters has appeared as one of the numerous meaningful and substantial explanations for exploiting renewable sources [7, 8]. Numerous sorts of high-step-up DC-DC converters are discussed. These structures are often classified into two categories: isolated and non-isolated classes employed in renewable energy usages [9, 10]. The isolated DC-DC converters employ a transformer to step up or step down the input voltage, whereas in the non-isolated DC-DC converters, this transformer is absent and the semiconductor devices are utilized to convert the voltage. So these types of converters have a more compact size, higher efficiency,

and lower production costs. In PV applications, a non-isolated DC-DC converter is employed as an input voltage converter that ranges from 12–60V to a fixed output voltage with a range that changes between 24V and 760V. A high-step-up DC-DC boost converter is demanded due to the high-output-voltage need with very restricted input voltage. Typical DC-DC converters produce a high voltage gain by a wide duty cycle. Conduction losses and electromagnetic interface (EMI) issues arise when the duty cycle increases [11, 12].

Additionally, the voltage gain in implementation is restricted because of the switches/diodes' power losses and the equivalent series resistance of capacitors and inductors. Switched capacitors and/or switched inductor units can be employed to improve the voltage gain [13, 14]. Likewise, as a result of high duty cycle levels, electromagnetic interface (EMI) challenges prevent voltage increase. At large voltage gains, however, the resulting peak current may cause a breakdown and reduce component lifespan [15, 16]. By altering the transformer's turn ratio, we may address these issues with different kinds of traditional DC-DC topologies like forward, fly-back, and push-pull structures. Nonetheless, the leakage inductance energy causes considerable voltage stress on the switches [17, 18]. Various high-gain converters based on coupled inductors with minimal core loss can be utilized. In these converters, the switches may function under demanding switching settings with large switching losses. The voltage gain of these structures is increased by adjusting the duty cycle of the switch and the turn ratio of the coupled inductor. The power switch may be subjected to short-term transient voltage, and the leakage effect of the coupled inductor limits voltage gain and results in substantial power losses [19, 20]. Isolated boost converters with a low peak voltage are presented. Nevertheless, the price and magnitude of these converters are significant due to their isolated construction. Non-isolated power converters can be employed to confound the challenges mentioned above. These structures equip

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diverse benefits, including cheap price and volume [21, 22]. The converter presented in [23] is a non-isolated type and appropriate for microgrid inverters. Nonetheless, the significant ripple of the input current lowers the input PV panel lifespan. A VMC and coupled inductor-based high step-up DC-DC is introduced in [24]. This converter has a significant input current ripple and the component count is enormous, resulting in lower efficiency. DC-DC converters with a considerable voltage gain are given in [25, 26]. Regardless, essential issues such as increased input current ripple, high peak voltage of semiconductors, diode reverse recovery, substantial element numbering, and low efficiency continue in the design of DC-DC converters. A switched inductor/capacitor-based transformer-less converter is raised in [27] which includes two switches resulting in substantial conduction losses. An expandable non-isolated DC-DC converter with high voltage gain and the ability to cancel input current ripple has been presented in [28], which can be used in PV systems. A coupled-inductor-based ultra-step-up DC-DC converter using the interleaved technique and having soft-switching capability is introduced in [29]. This structure utilizes a larger number of components and it does not share a common ground between the input and output ports. The converter based on a coupled-inductor and voltage multiplier cell is given in [30] in which the voltage gain is not considerable. Another high voltage gain DC-DC converter is presented in [31] which utilizes high component counts especially the passive elements. This case leads to an increase in the volume and size of the converter.

This research presents a high step-up converter by the use of VMC and coupled inductor for renewable energy applications, with improved efficiency and reduced blocking voltage across semiconductors. Employing a VMC and one coupled inductor causes the voltage gain of the proposed structure to be increased. In this topology, the only one used power MOSFET causes the cost of the converter to be diminished. The low component count and blocking voltage of the semiconductors are further advantages of this converter. Thanks to the presence of a VMC operating as a clamp circuit, the peak voltage across the switch can be reduced. As a result, a power MOSFET with a lower nominal voltage can be employed.

2. PROPOSED TOPOLOGY AND SWITCHING MODES ANALYSIS

The suggested converter is depicted in Fig. 1. This topology has ten elements including an inductor placed at the input side (L_{in}) to reduce its current ripple, a two-windings (n_1 and n_2) coupled inductor, three diodes (D_1 , D_2 , D_o), a power MOSFET (S), and four capacitors (C_1 - C_3 , C_o). D_1 and C_2 operate as a voltage clamp to reduce the peak voltage of S . The coupled inductor windings along with VMCs increase V_o with a small duty cycle. Based on the current of the switch and diodes, there are two main switching modes in each switching period (T_s) which are demonstrated in Fig. 2. The turn ratio of the coupled inductor is defined as $N = n_2/n_1$, and the used coupled inductor includes leakage and magnetizing inductances (L_k and L_m). The switching modes are analyzed in the following.

2.1. Switching mode 1 [$t_0 < t < t_1$]:

At the start of mode 1, S is turned ON by applying a gate-source pulse. L_{in} is started to charge via V_{in} . Therefore, the voltage of L_{in} is equal to V_{in} . On the other hand, the voltage of the primary side of the coupled inductor is negative resulting in decreasing i_{Lk} and i_{Lm} . D_1 and D_2 are reverse-biased while D_o is forward-biased. During this mode, C_1 , C_2 , and C_3 are discharged and C_o is charged. The equivalent circuit of this mode is depicted in Fig. 3 (a), and these equations are written:

$$V_{L_{in}} = V_{in}, \tag{1}$$

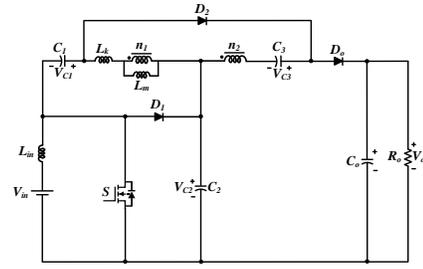


Fig. 1. The schematic of the proposed topology.

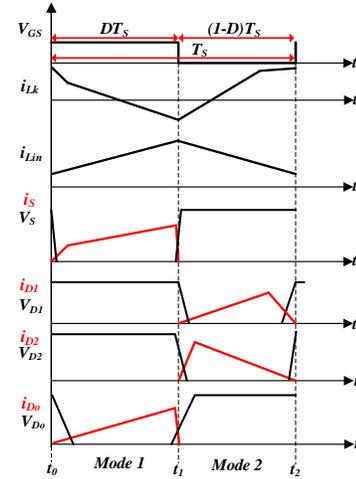
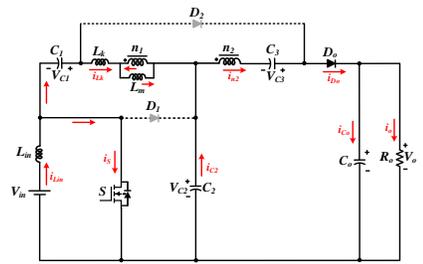
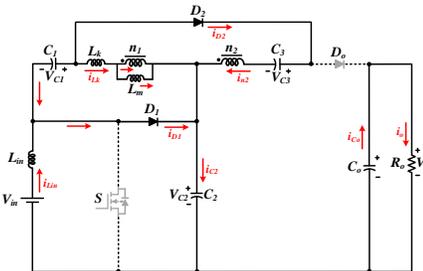


Fig. 2. The main waveforms.

$$V_{L_m} = V_{C_1} - V_{C_2}. \tag{2}$$



(a)



(b)

Fig. 3. The equivalent circuits, (a) Mode 1 and (b) Mode 2.

$$V_o = V_{C3} + V_{C2} - V_{n2}, \quad (3)$$

$$V_{n2} = NV_{Lm} = N(V_{C1} - V_{C2}), \quad (4)$$

$$i_{D_o} = i_{C_o} + i_o, \quad (5)$$

$$i_{n2} = -i_{C3} = i_{D_o}, \quad (6)$$

$$i_{L_{in}} = i_s + i_{L_k}. \quad (7)$$

2.2. Switching mode 2 [$t_1 < t < t_2$]:

At the start of mode 2, S is turned OFF. Thus, the voltage of L_{in} becomes negative, and its current is reduced linearly. Also, owing to the positive voltage on the primary side of the coupled inductor, i_{L_m} , and i_{L_k} are raised. During this mode, D_o is reverse biased, and D_1 and D_2 conduct. Because of current conducting by D_1 and D_2 , C_1 , C_2 , and C_3 are charged by stored energy in the coupled inductor's windings including leakage energy. Therefore, the leakage energy of the windings is recovered. Additionally, C_o is discharged to R_o . The current path of mode 2 is illustrated in Fig. 3 (b), and the following equations are calculated:

$$V_{L_{in}} = V_{in} - V_{C2}, \quad (8)$$

$$V_{L_m} = V_{C1}, \quad (9)$$

$$i_{D1} = i_{C1} + i_{L_{in}}, \quad (10)$$

$$i_{C3} = -i_{n2} = i_{D2}, \quad (11)$$

$$i_{C_o} = -i_o. \quad (12)$$

3. STEADY-STATE INVESTIGATION AND VOLTAGES CALCULATION

In order to facilitate the steady-state study of the converter, the leakage influence of the coupled inductor and parasitic resistance of the used elements have been neglected. Using the volt-sec equilibrium law over L_{in} , the voltage of V_{C2} can be calculated as Eq. (14):

$$\langle V_{L_{in}} \rangle_{T_s} = 0 \Rightarrow DV_{in} + (1-D)(V_{in} - V_{C2}) = 0, \quad (13)$$

$$V_{C2} = \frac{1}{1-D} V_{in}. \quad (14)$$

Applying the volt-sec balance principle on L_m , the voltage across capacitor V_{C1} is achieved:

$$\langle V_{L_m} \rangle_{T_s} = 0 \Rightarrow D(V_{C1} - V_{C2}) + (1-D)V_{C1} = 0, \quad (15)$$

$$V_{C1} = \frac{D}{1-D} V_{in}. \quad (16)$$

Based on Fig. 3 (b), V_{C3} can be defined versus V_{C1} :

$$V_{C3} = NV_{C1} = \frac{ND}{1-D} V_{in}. \quad (17)$$

Finally, using Eq. (3) and replacing V_{C1} , V_{C2} , and V_{C3} , V_o versus V_{in} (voltage gain $M = V_o/V_{in}$) is calculated:

$$\begin{aligned} V_o &= V_{C3} + V_{C2} - V_{n2} = V_{C3} + V_{C2} - N(V_{C1} - V_{C2}) \\ &= V_{C3} + (1+N)V_{C2} - NV_{C1} = \frac{1+N}{1-D} V_{in} \\ \Rightarrow M &= \frac{V_o}{V_{in}} = \frac{1+N}{1-D}. \end{aligned} \quad (18)$$

The peak voltage stress of D_1 and D_2 can be determined in switching mode 1. Based on this, the peak voltage of D_1 is:

$$V_{D1} = V_{C2} = \frac{1}{1-D} V_{in} \Rightarrow \frac{V_{D1}}{V_o} = \frac{1}{1+N}, \quad (19)$$

$$\begin{aligned} V_{D2} &= V_{C3} - (1+N)V_{L_m} = V_{C3} - (1+N)(V_{C1} - V_{C2}) \\ &= \frac{1+N-D}{1-D} V_{in} \Rightarrow \frac{V_{D2}}{V_o} = \frac{1+N-D}{1+N}. \end{aligned} \quad (20)$$

The peak voltage stress of S and D_o are calculated at mode 2, when these semiconductors are turned OFF:

$$\frac{V_S}{V_o} = \frac{V_{D1}}{V_o} = \frac{1}{1+N}, \quad (21)$$

$$\begin{aligned} V_{D_o} &= V_o - V_{C1} - V_{C2} = \frac{N-D}{1-D} V_{in} \\ \Rightarrow \frac{V_{D_o}}{V_o} &= \frac{N-D}{1+N}. \end{aligned} \quad (22)$$

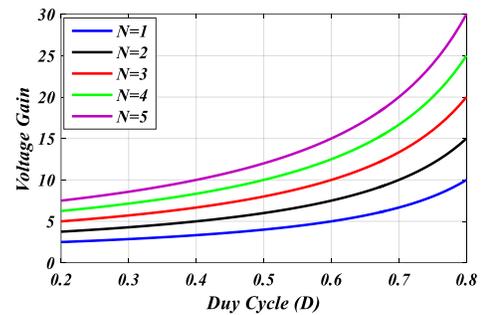
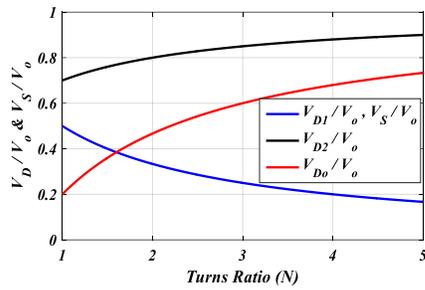
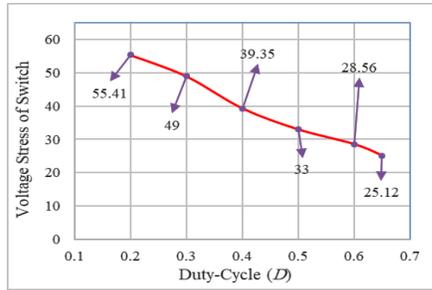


Fig. 4. The curve of voltage gain (M) in terms of duty cycle (D) for different values of turn ratio (N).

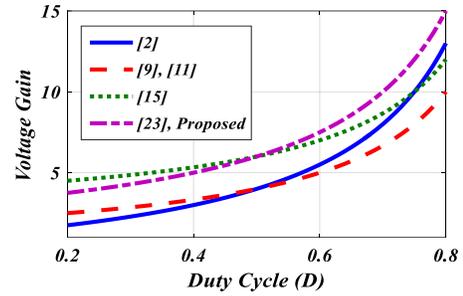
The variation of voltage gain versus diverse D and N is demonstrated in Fig. 4. Also, the normalized peak voltage of semiconductors versus turn's ratio number are pictured in Fig. 5 (a). According to this figure, for $N = 3$, the maximum normalized peak voltages of the semiconductors are lower than 0.86. Also, the peak voltage of S and D_1 is decreased as N increases. The voltage stress on the switch for a different range of duty cycles is indicated in Fig. 5 (b). This figure shows that the voltage stress throughout the switch is lower than the output voltage for all duty cycles, leading to higher efficiencies for such a converter.



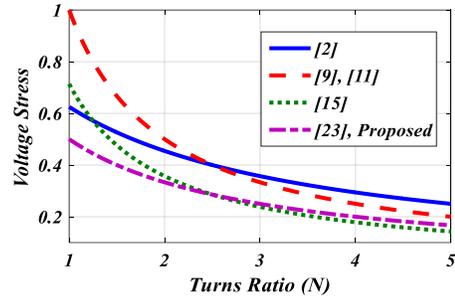
(a)



(b)



(a)

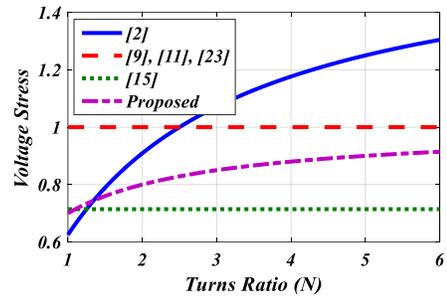


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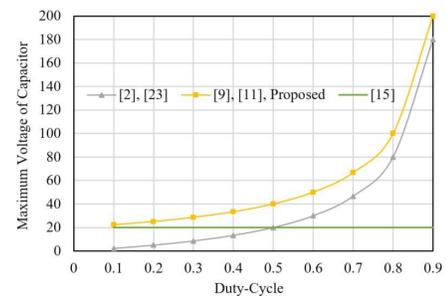
4. COMPARISON RESULTS

This section compares the proposed topology to that of other comparable converters. Table 1 provides a summary of this part. Based on this table, the number of used elements, voltage gain, peak voltage on switches/diodes/capacitors, size of the input current's ripple, cost, and power efficiency are taken into account. The device cost in the converters of Table 1 is almost the same. Converters in [11] and [15] use two power switches in their structures. However, in [15], only one magnetic core is used. Converters in [2] and [15] have higher diode counts, and the presented converter uses a higher number of capacitors. The entire components count in [9] is lower than others. But this topology endures high voltage stress on diodes and lower efficiency than the suggested converter. Voltage gain comparison is depicted in Fig. 6 (a). Based on this picture, the recommended topology and [23] benefit from superior voltage gain than others. The converter in [23], however, bears a large input current ripple. Therefore, it cannot be proper for renewable energy applications. Switches voltage stress comparison is demonstrated in Fig. 6 (b). The suggested topology and the structures in [23] and [15] have lower maximum peak voltage on the switches. Additionally, the diode voltage stress comparison is pictured in Fig. 6 (c). The topology in [15] has lower diodes maximum peak voltage. But for $N = 1$, the suggested topology and [15] have almost equal diodes peak voltage. The maximum voltage on the capacitors between the proposed converter and the others has been included in Table 1 and Fig. 6 (d). It is clear that the voltage stress of the capacitors for the proposed converter, [9], and [11] are higher than others. Table 1 illustrates the cost of the proposed converter and the other converters. By noticing Table 1, it is clear that [11] and [15] have higher costs than the proposed converter. The converters in [2] and [9] have approximately the same cost as the proposed converter. The number of cores and turns ratio value of the suggested converter can be decreased by increasing the power rating.

In addition, the nominal values of the power components are



(c)



(d)

Fig. 6. Comparison curves, (a) Voltage gain, (b) Switches voltage stress, (c) Diodes voltage stress, (d) Maximum voltage of the capacitors.

reduced by increasing the power rating, so it can be said that the proposed converter works in high power ratings with high efficiency and low cost (by choosing the suitable price of the power components). According to Table 1, the presented topology has higher power efficiency with a low input current ripple, high voltage gain, and low switch peak voltage. In light of these benefits, the designed converter is appropriate for applications involving renewable energy.

Table 1. Comparison results of the proposed topology.

Converters	Total Num. components	Num. components					Gain (M)	Max voltage on switches	Max voltage on diodes	Max voltage on capacitors	Cost (\$)	Eff [%]	Input Ripple
		C	Cl	L	D	S							
[2]	10	3	1	1	4	1	$(1+ND)/(1-D)$	$1/(1+ND)$	$N/(1+ND)$	$(NDV_{in})/(1-D)$	34.8	92.7	High
[9]	7	2	1	1	2	1	$N/(1-D)$	$1/N$	1	$(V_{in})/(1-D)$	31.8	95.9	Low
[11]	9	3	1	1	2	2	$N/(1-D)$	$1/N$	1	$(V_{in})/(1-D)$	47.8	95.5	Low
[15]	8	3	1	-	5	2	$N(2-D)/(1-D)$	$1/(2-D)N$	$1/(2-D)$	NV_{in}	44.8	92.9	High
[23]	8	3	1	-	3	1	$(1+N)/(1-D)$	$1/(1+N)$	1	$(NDV_{in})/(1-D)$	27.8	95.5	High
Proposed	10	4	1	1	3	1	$(1+N)/(1-D)$	$1/(1+N)$	$(1+N-D)/(1+N)$	$(V_{in})/(1-D)$	34.8	96.3	Low

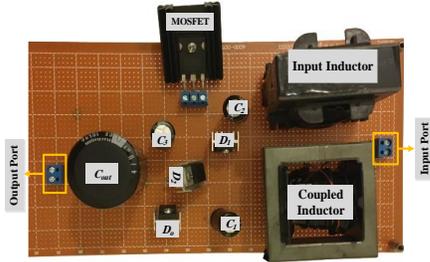
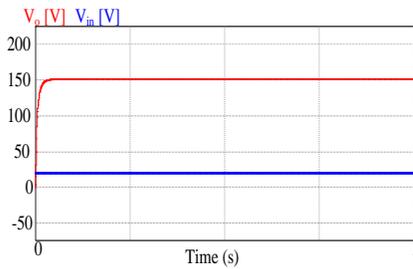
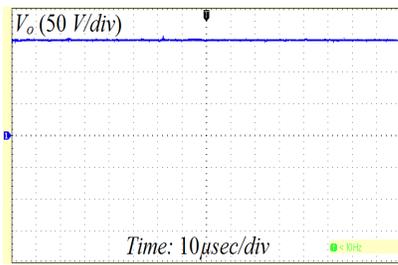


Fig. 7. Experimental prototype of the suggested converter.



(a)



(b)

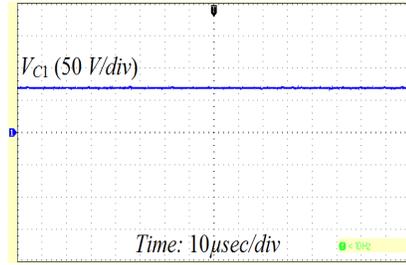
Fig. 8. Simulation and experimental waveforms of the output voltage; (a) Simulation result, (b) Experimental result.

5. SIMULATION AND EXPERIMENTAL RESULTS

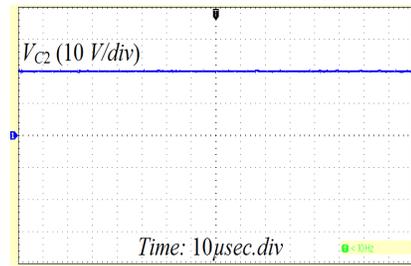
To prove the mathematical examination, the proposed converter is simulated in PSIM software and also its lab-scale is executed and experimented according to the parameters listed in Table 2. The experimental prototype of the converter is shown in Fig. 7.

The simulation results along with the experimental waveforms are given in Figs. 8-13. The simulation and experimental results of C_o voltage (V_o) are shown in Figs. 8 (a) and (b) which is fixed at 150V. Fig. 9 (a) shows that the voltage of C_1 is approximately 70V. It is transparent from Figs. 9 (b) and (c) that the voltage across C_2 and C_3 is about 20V and 50V, respectively.

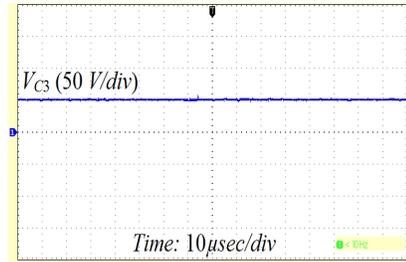
The simulation results of the capacitors voltage are shown in Fig. 9 (d). This figure confirms the experimental results. In Fig. 10, the voltage and current waveforms of the diodes D_1 and D_2 are demonstrated. Figs. 10 (a) and (b) demonstrate the simulation and experimental waveforms of D_1 voltage and current. These figures show that this diode's maximum voltage and current are



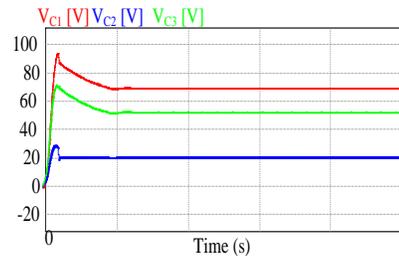
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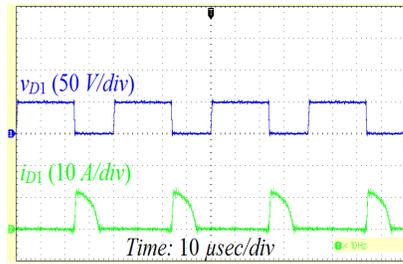
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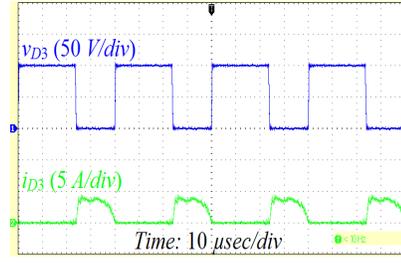
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Fig. 9. Capacitors voltage waveforms; (a) Experimental of C_1 , (b) Experimental of C_2 , (c) Experimental of C_3 , (d) Simulation of C_1 , C_2 , and C_3 .

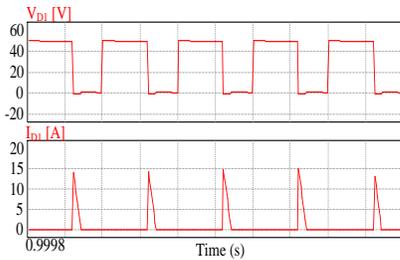
about 50V and 12A, respectively. As shown in Figs. 10 (c) and (d), D_2 experiences a maximum voltage and current equal to 100V and 2A, respectively. The simulation and experimental waveforms of the diode D_o and switch S are displayed in Fig. 11. According to Figs. 11 (a) and (b), when D_o is directly biased, its



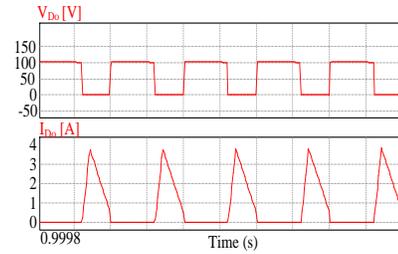
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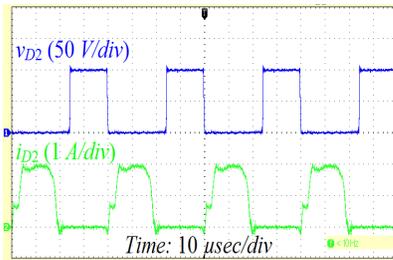
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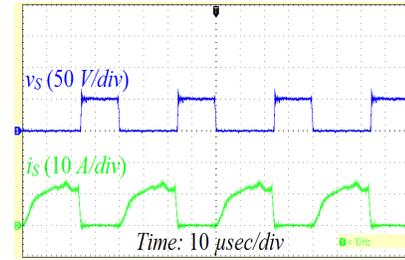
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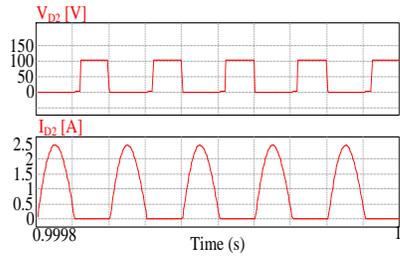
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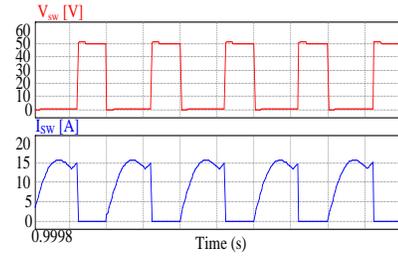
(c)



(c)



(d)



(d)

Fig. 10. Diodes D_1 and D_2 voltage and current waveforms; (a) experimental of D_1 , (b) simulation of D_1 , (c) experimental of D_2 , (d) simulation of D_2 .

Fig. 11. Diode D_o and switch S voltage and current waveforms; (a) Experimental of D_o , (b) Simulation of D_o , (c) Experimental of S , (d) Simulation of S .

maximum current is about 4A, and in the reverse-biased interval, the maximum voltage across it is 100V. For switch S in Figs. 11 (c) and (d), it is clear that the maximum voltage and current stresses are respectively 50V and 14A.

has been shown in Fig. 13. Based on this figure it is apparent that the proposed converter has higher efficiency when the output power is changed from light load to high load.

The inductor current waveforms are pictured in Fig. 12. The input inductor (L_{in}) current is demonstrated in Fig. 12 (a). Its average is about 8A and the peak-peak ripple is approximately 1A. So, $i_{L_{in}}$ is continuous and its ripple is almost 12.5%. The current waveforms of the primary and secondary sides of the coupled inductor are shown in Figs. 12 (b) and (c). As Fig. 12 (b) shows, $i_{L_{t1}}$ is a continuous current and its average is near zero. Further, the secondary side current ($i_{L_{t2}}$) waveform in Fig. 12 (c) is discontinuous. The efficiency curve of the proposed converter

6. CONCLUSION

This examination proposed a high step-up topology using VMC and magnetic coupling method with improved efficiency and reduced voltage stress on switches/diodes for renewable energy usage. Using a VMC and one coupled inductor, the proposed structure achieves a high voltage gain. In this converter, only one power MOSFET is employed, lowering the cost of the converter. Other benefits of this converter are its low number of devices and low blocking voltage of the semiconductors. Furthermore,

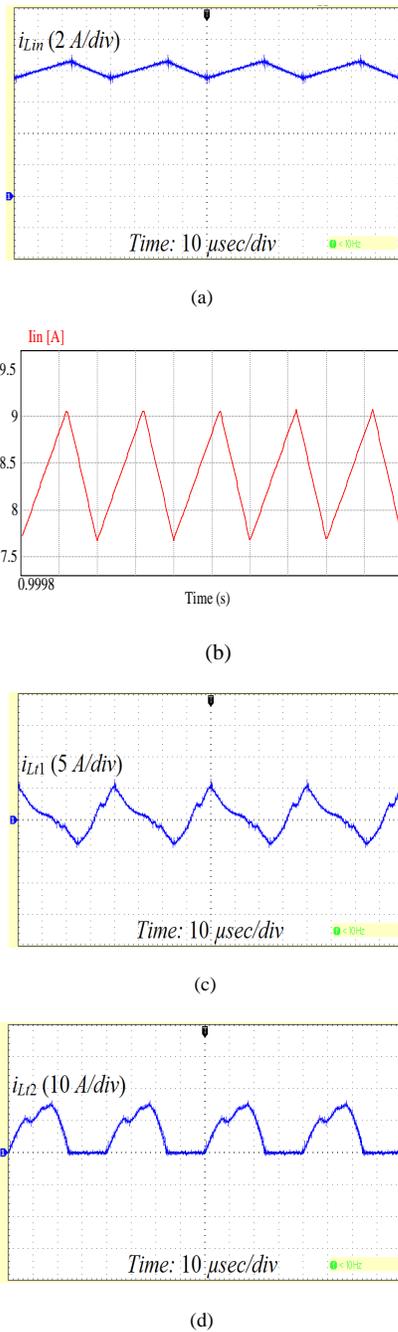


Fig. 12. Waveforms of the inductors current; (a) Experimental of L_{in} current ($i_{L_{in}}$), (b) Simulation of L_{in} current, (c) $i_{L_{t1}}$, (d) $i_{L_{t2}}$.

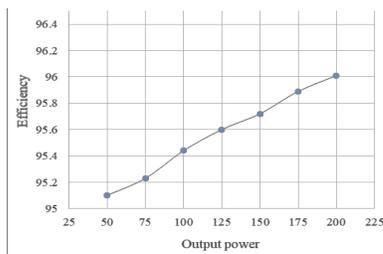


Fig. 13. Efficiency curve of the proposed converter versus output power.

Table 2. Specifications of the implemented converter.

Parameter	Value or part number	Parameter	Value or part number
P_o	200W	L_m	250 μ H
V_{in}	20V	L_{in}	500 μ H
V_o	150V	Switch	STW55NM60C
f_s	25kHz	Diodes	MUR2060
$N (N1/N2)$	2/1	C1-C3	100 μ F/200V
		C_o	470 μ F/450V

the VMC functions as a clamp circuit, reducing the peak voltage of the switch. As a consequence, in the presented converter, a low nominal voltage switch can be operated. The switching modes, steady-state study, and comparative study with other comparable converters are shown to demonstrate the performance and superiority of the converter. A 200 W experimental scale with a switching frequency of 50 kHz and a voltage conversion of 20V~200V is implemented to validate the mathematical equations.

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