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A Modified Clamp-Double Submodule (CD-SM) Based Modular Multilevel Converter (MMC) With Reduced Component Count for HVDC Application

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Abstract— *Recent grid codes require a high voltage direct current (HVDC) converter station remains connected and provide reliable operation under various faults. An improved clamp-double submodule (CD-SM) is introduced in this article, which belongs to the modular multilevel converter (MMC) topologies proposed for high voltage direct current (HVDC) systems. The proposed submodule (SM) topology features a reduced number of control switches, lower converter level faults, and DC fault-blocking capability compared to the conventional submodule topologies. A CD-SM consists of five IGBTs, two diodes, and two floating capacitors, where capacitor voltages are maintained according to the binary geometric propagation (GP) ratio which enables it to generate a maximum four-level output voltage. The hybrid pulse width modulation (PWM) technique is used to generate desired switching pulses for a converter and the associated voltage balancing control technique maintains the power exchange between the converters. In this article, the dimensioning of the proposed MMC converter, and its performance under different fault conditions is discussed in detail. Further, a quantitative comparison with other submodule topologies in terms of dc fault-blocking capability, output voltage level, and device count is discussed. Simulation in MATLAB/Simulink and their results validate the effectiveness of the proposed topology for MMC based HVDC system.*

Keywords—Modular multilevel converter (MMC), asymmetric clamp couble submodule (CD-SM), DC fault blocking capability, high voltage direct current (HVDC) system, reduced component count.

1. INTRODUCTION

With the increasing demand for electrical power and the growth of renewable energy sources, novel technologies are being researched to enhance electrical power transmission systems and guarantee the smooth integration of new electrical energy resources [1], [2]. Modular Multilevel Converters (MMCs) are broadly used in high-power and high-voltage applications like flexible AC transmission systems (FACTs), and HVDC transmission systems [3]. The MMC constitutes a large number of series connected submodules with similar structures. This Converter has gained notable popularity due to distinctive advantages including low filtering requirements and modularity [4], [5]. A rising interest in reliability analysis and fault-tolerant capabilities has been inflamed by the broad use of converters in high-voltage and high-power electrical systems. In general, the system-level faults of an MMC converter can be classified as converter-level faults, DC-side faults, and AC-side faults [6]. Several literature studies address AC-grid faults by employing several control strategies such as fault current limiters, relays, and AC breakers [7], [8]. The converter level faults are inclined to all power electronic converters and because of a higher number of components in MMC converters, the problem is more severe resulting in higher points of failure. Hot-swap features and redundant sub-modules can be used as a solution to a converter-level fault [9–11].

One of the most challenging fault situations is DC short circuit faults for the voltage source converter-based high voltage DC (VSC-HVDC) transmission, mainly when the overhead transmission lines are employed to transmit DC power. Protection schemes are required to look after a safe MMC operation against DC short circuit faults [12]. Conventionally a half-bridge sub-module (HBSM) is used in MMCs. However, the lack of fault ride-through capability put restrictions on the use of HBSM-MMC [13]. To address this challenge various protection schemes were investigated in the literature. To improve the converter reliability the thyristor devices are used commonly in parallel with the IGBT-based HBSM [14]. All the power switches are turned off and parallelly connected thyristors are turned on during a DC fault. Hence, the submodules are bypassed by thyristors and protected against a DC fault. However, the AC feeding phenomenon does not cut off by this approach. Another method is to use submodules with fault-ride-through capability in MMCs to improve their performance of it under DC fault conditions [15]. In [16], various protective submodule (SM) topologies such as clamp double (CDSM), hybrid double, full-bridge (FBSM), series connected double (SCDSM), active clamp T-type (ACTSM), and clamp circuit double submodule (CCSM) have been proposed. The above-mentioned topologies not only diminish efficiency by increasing power losses but also add control complexity [16].

To solve the above-mentioned issues geometric propagation (GP) ratio-based asymmetrical approach is applied to conventional clamp-double submodule (CD-SM) in which asymmetric capacitor voltage as per 1:2 (binary GP ratio) is maintained across the submodule capacitors. It makes it possible to generate a higher number of output voltage levels by appropriate selection of capacitor voltage magnitude without making changes in the converter circuit [17]. The asymmetric clamp-double submodules (CD-SM) allow for utilization of the advantage of more output levels with less number of switches hence less number of floating

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capacitors and voltage sensors are required. Also, it provides DC fault blocking capability and enables MMC to deal with low DC voltage operation, DC short circuit fault ride through, and the black starting hence the reliability can be enhanced by connecting several modules in series. In this article, asymmetrical clamp-double submodules (CD-SM) based modular multilevel converter (MMC) topology is proposed.

A hybrid modulation technique is used to generate gating signals for control switches to obtain different voltage levels, utilizing an asymmetric CD-SM of the MMC [17–19]. A modified voltage balancing algorithm, where the voltages across the capacitor of each CD-SM are measured using voltage sensors and normalized then sorted to aid in voltage balancing [17, 20]. This voltage balancing algorithm improves performance by reducing the capacitor voltage ripple compared to the conventional voltage balancing algorithm. In this study, a 3-ϕ A-MMC having two SMs in each arm is simulated using MATLAB-Simulink to generate a maximum 13-level output voltage and 25-level output voltage with carrier interleaving using a binary geometric propagation (GP) ratio. Detailed simulation results are illustrated which show the figure of the output currents and voltages with or without interleaving angle. A comparison of proposed asymmetric CD-SM with conventional SMs having the same number of output voltage levels is also shown to illustrate the additional advantages of such MMCs.

The remainder of this article is organized as follows. Section II introduces the modified clamp-double sub-module-based (CD-SM) MMC topology and describes the circuit and its working. The hybrid modulation technique, capacitor pre-charging process, and voltage balancing (VB) algorithm are summarized in Section III. Simulation results by considering two modules per arm and a comparison of the proposed topology with conventional SMs are described in Section IV and the article concludes in Section V.

2. CIRCUIT TOPOLOGY AND ITS DESCRIPTION

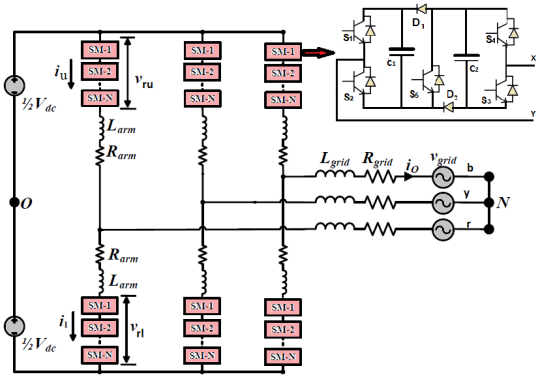


Fig. 1. The circuit configuration of asymmetric clamp double submodule (CD-SM) based MMC.

The asymmetric clamp-double SM-based MMC illustrated here in this article allows using a novel asymmetric SM with traditional MMC topology. A 3-ϕ structure of the proposed converter topology is shown in Fig. 1. Each leg comprises two arms in the MMC, having n series-connected SMs in both arms and by appropriate switching of the SMs required output voltage can be generated. Consider the r-phase, for example, the relationship among AC, DC, and arm voltage is shown as (1), where v_{rl} and v_{ru} are the lower and upper arm sub-modules output voltage, v_r is the r-phase voltage, V_{dc} is the DC bus voltage and V_{dc-} and V_{dc+} are the negative and positive phase to ground voltage.

$$\begin{aligned} v_{ru} &= \tfrac{V_{dc}}{2} - v_r - L\tfrac{di_{ru}}{dt} \\ v_{rl} &= \tfrac{V_{dc}}{2} + v_r - L\tfrac{di_{rl}}{dt} \\ V_{dc+} &= |V_{dc-}| \end{aligned} \tag{1}$$

The relationship among arm current, AC, and DC is illustrated as:

$$\begin{aligned} i_r &= i_{ru} - i_{rl} \\ i_{dc} &= i_{ru} + i_{yu} + i_{bu} \end{aligned} \tag{2}$$

The internal architecture of the asymmetric clamp-double submodule (CD-SM) is also shown in Fig. 1. As can be seen, it comprises two capacitors C_1 and C_2 in binary configuration, C_1 and C_2 are maintained at asymmetric voltages of V_c and $2V_c$ respectively. $CD-SM$ consists of five IGBTs, two power diodes, and two asymmetric capacitors. In asymmetric CD-SM based MMC with binary geometric propagation (GP) ratio, it is possible to generate maximum four-level output voltage (0, V_c, $2V_c$, $3V_c$) by appropriate switching of the switches $S_1 - S_5$ of a submodule as per equation (3). The DC-link voltage V_dc can be related to the submodule capacitor voltage V_c as per (4):

$$V_{xy} = (S_1.S_4.S_5).V_c + (S_2.S_3.S_5).2V_c + (S_1.S_3.S_5).3V_c \tag{3}$$

$$n.V_c + n.2V_c = V_{dc} \Rightarrow V_c = \frac{V_{dc}}{3n} \tag{4}$$

Table 1 shows the different switching signal combinations and the related voltage level generation from an asymmetric clamped double submodule (CD-SM) to generate a four-level output voltage using a binary ratio. The positive current direction is defined such that it charges the capacitors in its path whereas the negative current discharges them. As can be seen, the proposed module configuration allows for the generation of a maximum of four distinct voltage levels: 0, V_c, $2V_c$, and $3V_c$. This is an improvement over the conventional MMC symmetrical clamp double submodule which can generate only three levels. During normal operation, when both capacitors are bypassed, the current flows through S_2, S_4, and S_5 (Fig. 2-(a)). When S_1, S_4, and S_5 switches are turned on, the C_1 is inserted and SM generates V_c voltage (Fig. 2-(b)).; if s_2, s_3 and s_5 are turned on, the C_2 is inserted and SM generates $2V_c$ voltage (Fig. 2-(c)). If s_1, s_3, and s_5 are on-state, both capacitors are inserted and the SM generates $3V_c$ voltage. (Fig. 2-(d)). As soon as the fault occurs, all control switches in the submodules are turned off. If the current flows from X to Y or Y to X, the equivalent circuit is that two capacitors are charged and connected in series or parallel respectively. Then the counter-emf is built up and the fault current can be cut off.

By using asymmetric CD-SM, to generate a maximum number of output voltage levels, requirements of IGBTs, diodes, and capacitors can be obtained from equation (5)- (7) respectively, where n is the number of SMs.

$$N_{level} = 3n + 1 \tag{5}$$

$$N_{IGBT} = 5n \tag{6}$$

$$N_{Diode,cap} = 2n \tag{7}$$

3. MODULATION AND CONTROL OF PROPOSED MMC

In each submodule of the $A-MMC$, there is a capacitor voltage asymmetry, since they are made from two half-bridges connected using a control switch, one at V_c volts and the other at $2V_c$ respectively. Hence, each module can generate a maximum of four output voltage levels in proposed MMC as per the GP ratio between the capacitor voltage of a submodule. Uneven loss distribution among the submodules is the main disadvantage of the level-shifted modulation, which is undesirable for the MMC.

Table 1. Switching states for an asymmetric clamp-double sub-module.

V_{xy}	S_1	S_2	S_3	S_4	S_5	I	V_{cl}	V_{c2}
0	0	1	0	1	1	≥ 0 OR <0	=	=
V_c	1	0	0	1	1	≥ 0	↑	=
						<0	↓	
$2V_c$	0	1	1	0	1	≥ 0	=	↓
						<0		↑
$3V_c$	1	0	1	0	1	≥ 0	↑	↓
						<0	↓	↑

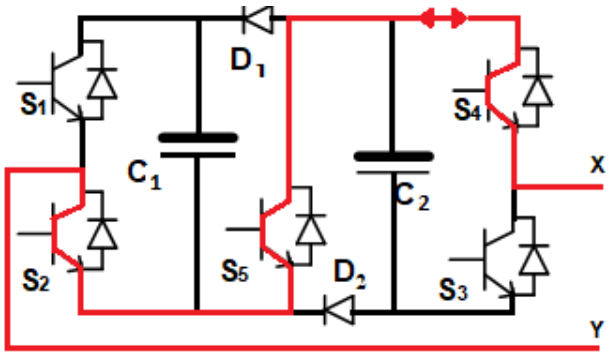
Switches $S_1 - S_5$ contain IGBT and reverse connected diodes, and ↑, ↓ and = indicates states of charge of the cell capacitors (discharge, charge, and unchanged) for the distinct polarity of arm current.

A phase-shifted modulation technique for MMC will result in some mismatch pulses in the output voltage of submodules [21]. A combination of level-shifted and phase-shifted pulse width modulation, called the hybrid PWM technique is used for proposed MMC [20]. In Hybrid PWM, in the context of a single CD-SM with binary GP ratio between capacitor voltage of a submodule, a group of three level-shifted carriers are first stacked on top of one another and three phase-shifted triangular carriers come into play. Hybrid PWM can also be utilized with carrier interleaving in proposed MMC to obtain higher output voltage levels. For an odd number of submodules, there will be a 00 phase displacement, and for an even number of submodules 1800 phase displacement between carriers.

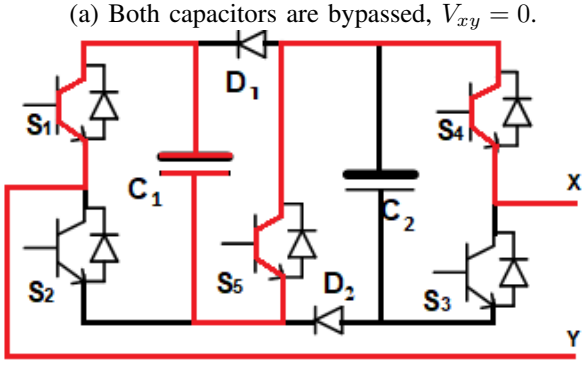
In this article, two sub-modules in each arm are used to construct proposed MMC and driven by the Hybrid PWM technique. For MMC based on binary GP ratio, three groups of stacked carriers are used. For each phase of the A-MMC, these hybrid triangular carriers are compared with v_u (upper arm) and v_l (lower arm), two normalized sinusoidal references to synthesize the output voltage.

For proper operation of the proposed MMC and to restrict the circulating current, two floating capacitors of a submodule need to be balanced at voltage V_c and $2V_c$. The voltage balancing technique based on normalization [20] has been modified when it is used with the proposed MMC. This normalization is done as per $V_{c2}/2$ for capacitor rated $2V_c$. The decision of which submodule to insert/remove is done once the normalized values are computed and also it depends on the direction of the current flow [20]. As per Table 1, a positive current direction charges the capacitor and the negative current direction discharges it. The capacitor voltage remains unaffected if the submodule is bypassed. Using the realization of the direction, then the capacitor which is farthest from the normalized rated value is selected. The modulation will demand only one level to be inserted/removed at a time. Thus, as a case, the addition/subtraction of a voltage level in an arm can be done according to the voltage balancing algorithm based on normalization as shown in Fig. 4 [20].

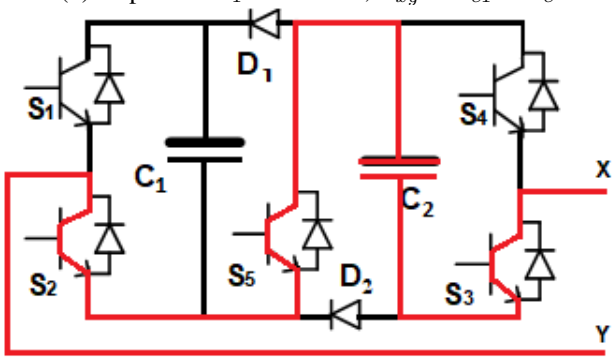
In MMC, the submodule (SM) capacitors should be pre-charged to their nominal voltage during the startup process [22]. To pre-charge capacitors of the asymmetric CD-SM at appropriate V_c and $2V_c$ voltage levels with binary GP ratio PWM technique is used in this article. During the pre-charge time, a resistor connected in series is used in a DC-bus path to keep the charging current low and it can be bypassed with a circuit breaker after the pre-charge process is complete. Based on the RC time constant capacitors voltage slowly increases and hence all the capacitor starts to get charged. The voltage sensors keep a check on the capacitor voltages and give input to a controller. As soon as the capacitors of each cell obtain the reference voltage value a controller restricts gate pulses to the cell. To prevent the load current identical number of cells must be inserted during the whole pre-charge process. All the capacitors C_{1n} are inserted at the primary stage of the pre-charging process. At that time the capacitor C_{2n} is all bypassed. All the capacitor C_{1n} start getting charged and the slow increment in their voltage depends on the RC time constant. The primary stage of this pre-charging sequence ensures that all the capacitors C_{1n} get charged to $V_dc/3n$. In a later stage, all the capacitor C_{1n} are bypassed. In the later stage of this pre-charging sequence make sure that all the capacitors C_{2n} get charged to $2V_{dc}/3n$. To ensure the capacitors are subjected equally to the charging current and get charged at the same voltage level.



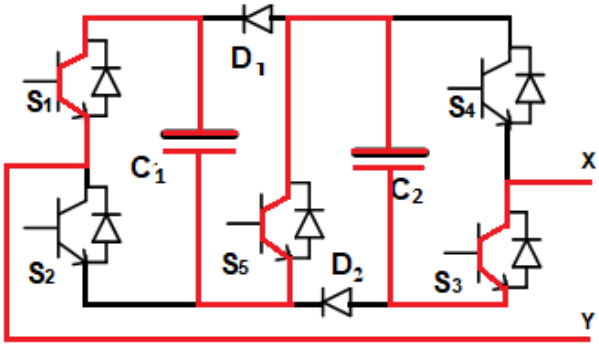
(a) Both capacitors are bypassed, $V_{xy} = 0$.



(b) Capacitor C_1 is inserted, $V_{xy} = V_{c1} = V_c$.



(c) Capacitor C_2 is inserted, $V_{xy} = V_{c2} = 2V_c$.



(d) Inserted both capacitors, $V_{xy} = V_{c1} + V_{c2} = 3V_c$.

Fig. 2. Structure and working process of asymmetric clamp-double submodule.

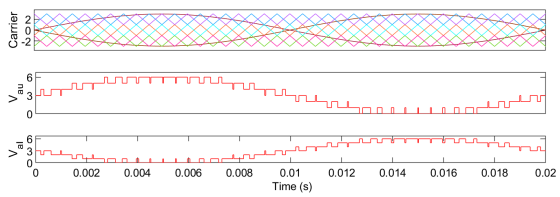


Fig. 3. Hybrid Modulation technique for asymmetric CD-SM based MMC.

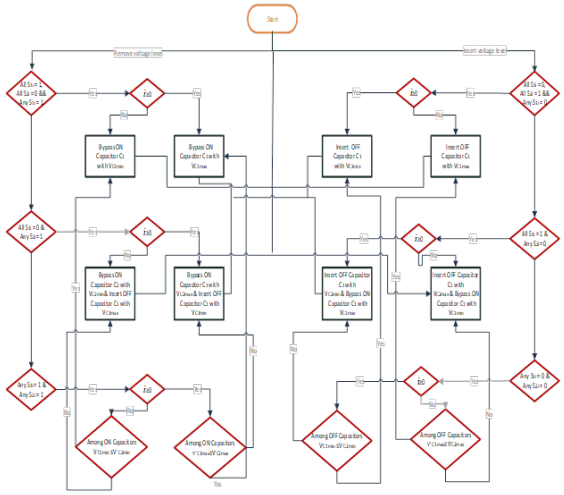


Fig. 4. Modified voltage balancing (VB) algorithm (for Binary GP ratio of capacitor voltage in a submodule).

4. SIMULATION MODEL AND THEIR RESULTS

The 3-phase MMC with asymmetric CD-SM submodule was simulated in MATLAB/Simulink having four submodules per phase and driven with hybrid PWM. A 9 kV stiff DC voltage source is used as a DC bus and three legs of the proposed converter are connected to the AC grid. Each submodule is equipped with two voltage sensors to measure capacitor voltage and each arm is having one current sensor to sense the direction of the current. The outputs of the voltage sensors and current sensors are fed to the voltage balancing block. The normalized sinusoidal reference is used with hybrid modulation for power transfer. Pulses are then generated, corresponding to each submodule in the entire phase leg. These pulses are then passed through the digital decoder logic, to generate individual pulses for the submodules. Table 2 illustrates the parameters used for the simulation.

For a 9 kV DC bus, the individual capacitor voltage rating with binary GP ratio is 1500 V and 3000 V for C_1 and C_2, respectively as derived from Equation (4). The optimal capacitance value depends upon the highest discharging period, lowest voltage ripple (V), and peak load current values [23, 24]. In a proposed MMC, it has two pairs of capacitors having an actual capacitance of $C/3$ and $2C/3$ respectively, in each arm. Assuming $C_2 = 1.5 * C_1$ to do charge balance, compared to capacitance C per cell of the traditional MMC, proposed MMC requires capacitance of $5C/9$ for C_1 and $5C/6$ for C_2. Therefore, concerning to 10 mF of capacitance required in each cell of the traditional MMC, the proposed structure of MMC requires 5.55 mF and 8.33 mF capacitance, respectively. In A-MMC lesser number of submodules is required, and fewer semiconductors conduct as compared to a conventional MMC, resulting in lower switching losses and conduction losses which are also benefited from the hybrid PWM technique.

The proposed MMC can generate a maximum thirteen-level output voltage per phase without carrier interleaving and twenty-five-level output voltage per phase with carrier interleaving, using two asymmetric CD-SM submodules in an arm. It requires a total of ten IGBTs and four diodes per arm, two capacitors of V_c voltage, and two of $2V_c$ voltages. In proposed MMC it is possible to obtain a higher number of output voltages levels using the same number of cells with using an interleaving angle in the hybrid modulation technique. Hybrid PWM can also be deployed with similar carrier interleaving, with the proposed MMC using binary GP ratio, to generate $3n+1$ to $6n+1$ output voltage levels.

Table 2. Simulation parameters.

Parameters	MMC
Submodules/phase	4
Output frequency	50 Hz
Switching frequency (f_s)	1 kHz
Arm resistor R_a	0.1 Ohm
Arm inductor L_a	1 μH
DC bus voltage V_{dc}	9 kV
Submodule capacitor C_1	5.66 mF
Submodule capacitor C_2	8.33 mF
Modulation technique	Hybrid PWM

The first set of simulation results as shown in Fig. 5 as (a & b) shows the 13-level output voltage and its THD of 15.81%, (c & d) shows the output current and its THD of 9.81% respectively using a hybrid modulation technique without interleaving angle and having two submodules per arm. Fig. 6-(e) shows the capacitor voltages of SMs which are nearly balanced at voltage V_c and $2V_c$. This is observed in the capacitor voltages for the V_c in SMs having higher ripple content than capacitors with $2V_c$. Fig. 6 shows the 25-level output voltage with THD 8.74%, output current with THD 7.07%, capacitor voltage, and harmonic spectrum of output voltage and current using a hybrid modulation technique with an interleaving angle having the same number of submodules per arm. From the illustrated Fig. 6-(e) the capacitor voltage ripples are less and within the permissible limit. The output voltage and output current synthesized have very low THD content in asymmetric CD-SM-based MMC using carrier interleaving compared to without carrier interleaving. Though the above results are acceptable, an investigation needs to be done on capacitor voltage balancing throughout the range of power factor cos ϕ and modulation index (m) to suggest a suitable stability region with the proposed modulation and voltage balancing strategy.

To check the dynamic performance and the efficacy of the modified voltage balancing algorithm various faults like L-G, L-L-G, and L-L-L-G are applied from 0.06 s to 0.1 s to the proposed MMC. The L-G fault is applied at $t = 0.06$ second to 0.1 seconds as in Fig. 7-(a) and the system gets stabilized within 2-3 cycles after the fault is removed. Fig. 7-(b) shows that when the L-L-G fault is applied the balancing algorithm works satisfactorily but it requires 4-5 cycles to get stabilized. As can be seen in Fig. 7-(c)–(d) that after L-L-L-G faults the system recovers faster than the above-mentioned fault conditions. These results verify the performance of the proposed MMC with a modified voltage balancing block. Hence, from the above, it is said that the modified voltage balancing (VB) block and proposed MMC is performing better under abnormal conditions. A comparison of THD of output voltages and currents concerning modulation index is illustrated in Figs 8-(a) and (b) respectively. From that, it is verified as the modulation index increases THD decreases, and capacitor ripples are also within permissible limits.

To evaluate efficiency, losses were calculated with varying output power (P_o) having constant switching frequency (f_{sw}) and then the losses are converted on per unit ($p.u.$) basis. Fig. 9 shows the P_{sw} rises linearly and Pcond. becomes steeper concerning output power (P_o). In the proposed MMC, Pcond. becomes steeper

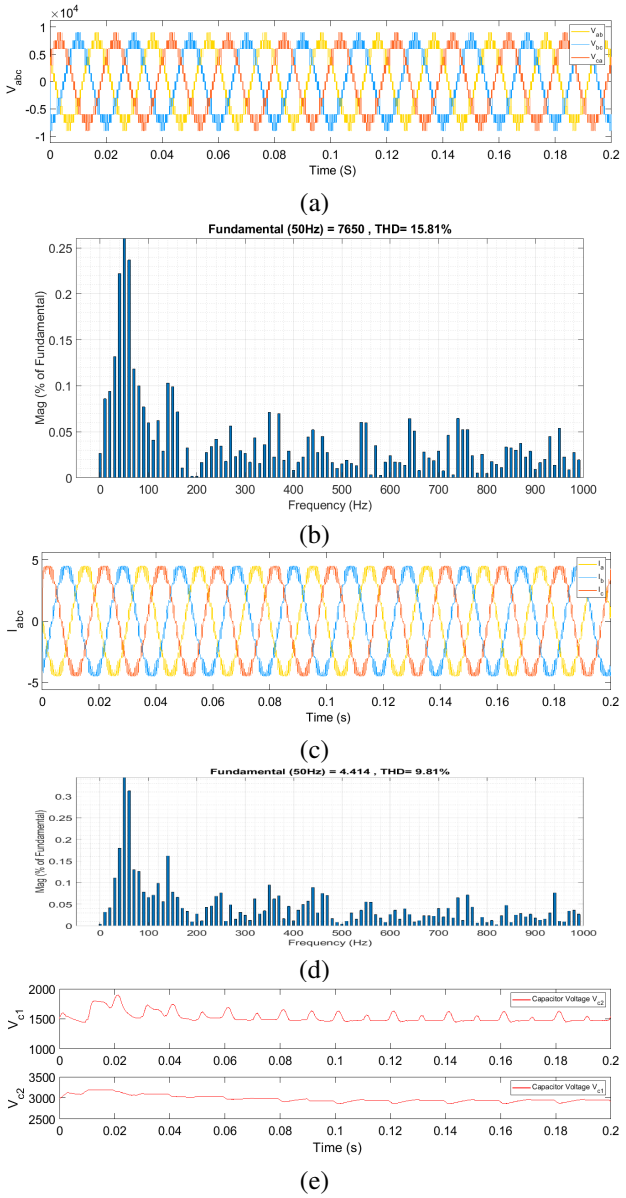


Fig. 5. Simulation results of asymmetric CD-SM based MMC with binary GP ratio and without carrier interleaving (a) O/P voltage V_{abc}, (b) O/P voltage THD, (c) O/P current I_{abc}, (d) O/P current THD, and (e) Capacitor voltage.

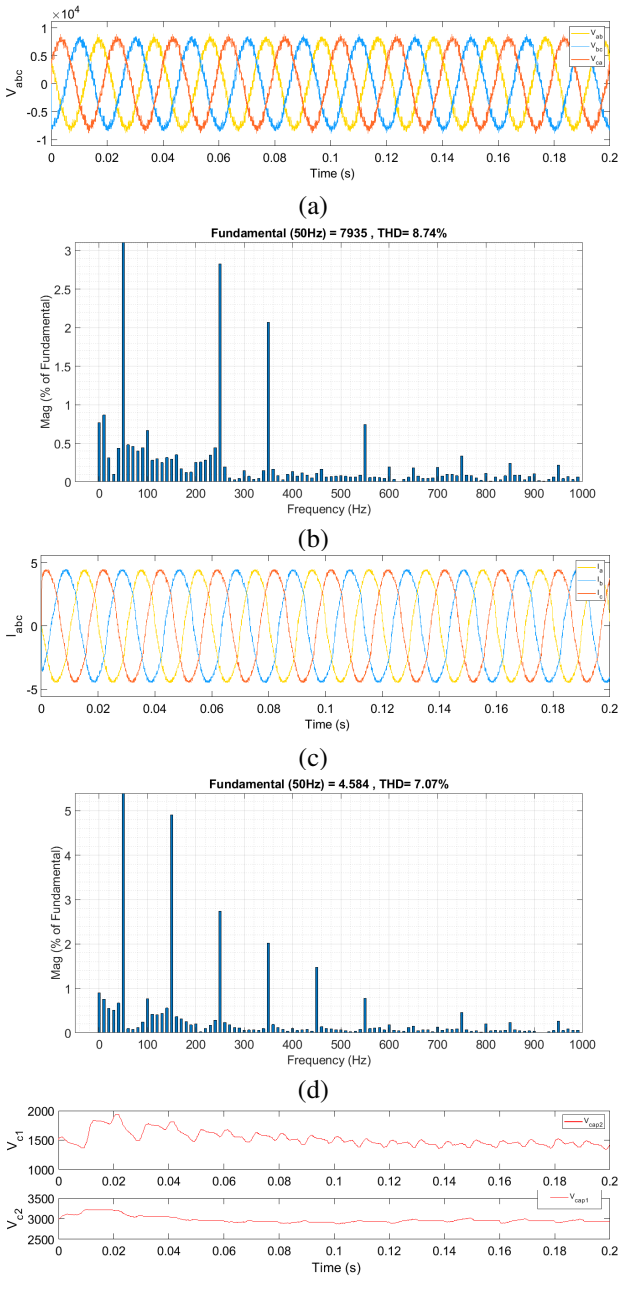


Fig. 6. Simulation results of asymmetric CD-SM based MMC with binary GP ratio and with carrier interleaving (a) O/P voltage V_{abc}, (b) O/P voltage THD, (c) O/P current I_{abc}, (d) O/P current THD, and (e) Capacitor voltage.

as P_o rises because of lesser submodules. On the other hand, the switching energies rise linearly over the range of P_o.

An exhaustive scientific comparison among different existing traditional symmetrical cell topologies and novel asymmetrical submodules is presented in Table 3. From that it can be seen, to obtain an equal number of output voltage levels the symmetrical half-bridge and full-bridge require three times the number of SMs concerned with asymmetrical SMs, as they can generate only two levels of output voltage. If DC fault handling capability is a must, mixed cell SMs, full-bridge SMs, and clamp-double SMs can be used. In a physical hardware model, additional components like bypass switches and protection thyristors are required for maintenance and safety. Also connecting submodules requires high current-carrying busbars. As can be seen that use of asymmetric SMs reduces the requirements of such components as illustrated in Table 3 and Fig. 10. A lesser control switch requires a lesser number of gate drivers, which can reduce the capital cost and overall size of the HVDC system. It also increases its reliability, and compactness and reduces complexity. As can be seen from Table 3, capacitors with different voltage ratings are used in the same submodule hence unequal-rated control switches have to be used. Also, the requirement of a number of asymmetric SMs is less compared to symmetrical SMs, which results in a higher device stress in asymmetric SMs.

The asymmetric HB-SM has a simple design, easy control, low power losses, and high efficiency but does not provide bipolar operation and DC fault blocking. The asymmetric FB-SM has twice the number of control switches as the asymmetric HB-SM for the same voltage rating. In FB-SM, during normal operation, four devices are conducting at a time resulting in higher power losses and lower efficiency but it can generate negative voltage

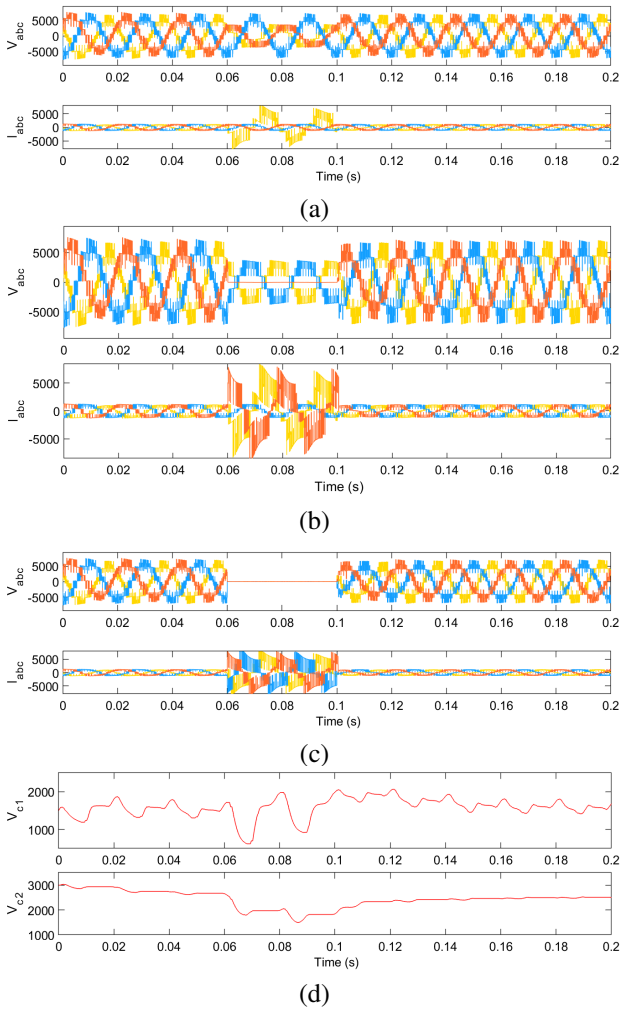


Fig. 7. Simulation results of asymmetric CD-SM based MMC under (a)line-to-ground (L-G) fault, (b) line-to-line-to-ground (L-L-G) fault, (c) line-to-line-to-line-to-ground (L-L-L-G) (d) Capacitor voltage under the faulty condition.

hence it can limit DC fault current. A combination of HB-SM and FB-SM, known as mixed-cell possesses DC fault-blocking capability. During normal operation, three switches are conducted out of six switches resulting in a lesser efficiency compared to asymmetric HB-SM and higher efficiency compared to asymmetric FB-SM. The CD-SM is formed by two half-bridges with an additional two diodes and a control switch. This topology can limit the current during DC side faults. The power losses, efficiency, and design complexity are significantly low compared to asymmetric FB-SM and Mixed-cell. In the HVDC system, protection against the DC side fault is desirable. Asymmetric CD-SM performs better than other asymmetric SMs that possess DC fault-blocking capability. Overall, the asymmetric CD-SM-based MMC proves to be a good choice for a modular structure to be used in future HVDC applications. Also, this asymmetrical CD-SM-based MMC topology provides some essential superiority like a reduced number of control switches, lower converter level faults, and DC fault-blocking capability which makes it a viable candidate, to be considered as an alternative to the conventional MMC. Assuming generating the same number of output voltage levels of 2n+1 per leg of the MMC.

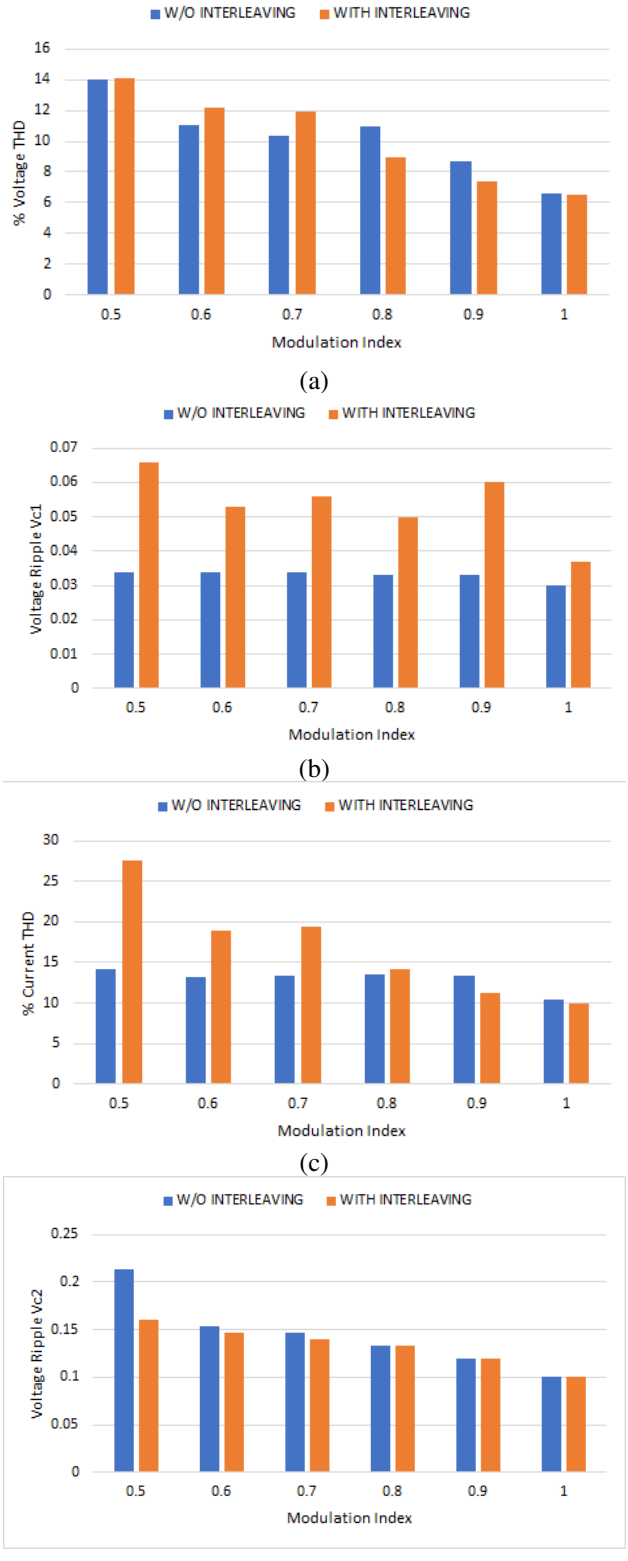


Fig. 8. Variation with modulation index (m) of (a) O/P voltage THD, (b) O/P current THD, (c) Capacitor voltage ripple of V_{c1}, (d) Capacitor voltage ripple of V_{c2}.

5. CONCLUSION

DC-side fault blocking capability with a reduced component count in MMC is a major challenge. In this article, the

Table 3. Comparison of proposed submodule topology with other topologies.

Parameters	Types of submodules						
	Half-bridge (HB) [25]	Full-bridge (FB) [25]	Clamp-Double (CD) [26]	Asymmetrical Half-bridge (A-HB) [20]	Asymmetrical Mixed cell [27] Binary GP	Asymmetrical Full-Bridge (A-FB) Binary GP	Asymmetrical Clamp-Double (A-CD) Binary GP
Fault handling	No	Yes	Yes	No	Yes	Yes	Yes
Control complexity	high	highest	highest	Lowest	Low	Low	Low
Trinary Operation	No	No	No	No	Yes	Yes	No
No. of submodule*	2. n	2. n	n	0.66 n	0.66 n	0.66 n	0.66 n
No. of IGBT's	4. n	8. n	5. n	2.64 n	3.96 n	5.38 n	3.3 n
No. of Gate drivers	4. n	8. n	5. n	2.64 n	3.96 n	5.38 n	3.3 n
Semiconductors in current paths	2. n	4. n	3. n	1.5. n	2.25 .n	3. n	2.25 .n
Voltage stress	V_{dc}/n	V_{dc}/n	V_{dc}/n	V_{dc}/n	V_{dc}/n	V_{dc}/n	V_{dc}/n
No. of busbars	2 .n	2 .n	N	0.75 .n	0.75 .n	0.75 .n	0.75 .n
Semiconductor losses	=	highest	Moderate	Lowest	high	Moderate	Low

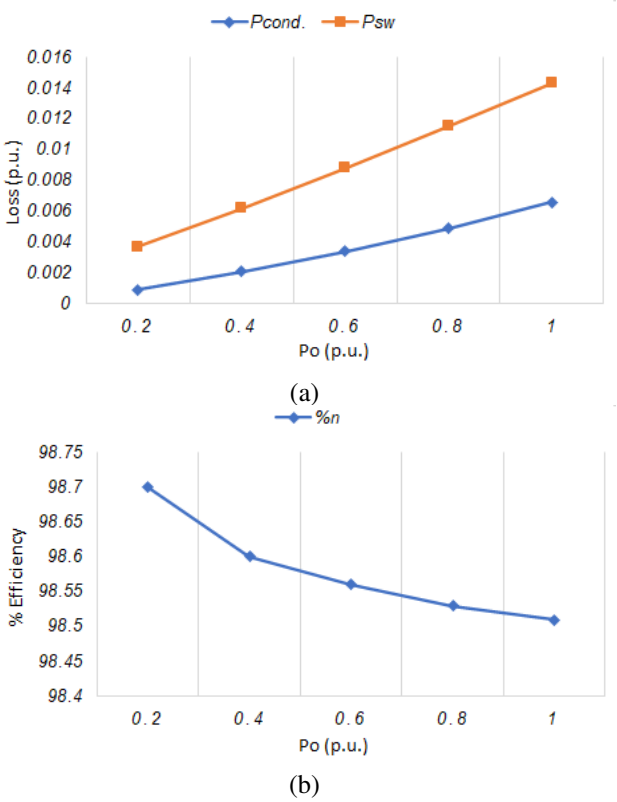


Fig. 9. (a) Variation of conduction and switching losses with output power; (b) Variation of efficiency with output power.

asymmetric clamp-double submodule (CD-SM) based MMC has been projected as a converter with a reduced component count, lower converter level faults, and DC fault-blocking capability. To control its operation, a modified voltage balancing (VB) algorithm and hybrid pulse width modulation has been illustrated and successfully verified with asymmetrically charged capacitors of the submodule. Through simulations in MATLAB/Simulink, the operation of the asymmetric clamp-double submodule (CD-SM) based MMC and its effectiveness were confirmed. A comparative study of the proposed topology, newly developed topology, and traditional topologies was done and the proposed topology performed superior, in terms of efficiency and improved DC fault-blocking capability. An analytical circuit component counts comparison among different submodule topologies was also done and the asymmetric HB-SM was found superior to others but does not possess DC fault-blocking capability. The proposed topology requires the least number of components compared to others who possess DC fault-blocking capability, hence the occurrence of converter-level faults can also be the least. Though the higher device stress and unequal ratings of control switches are some of the limitations of asymmetric SMs. The performance of the proposed MMC was found better for other parameters like capacitor voltage ripple, circulating current, output current, and voltage THD. From this, it is said that asymmetric CD-SM-based MMCs will be a viable alternative to the traditional MMCs in future HVDC implementation having a more compact, reliable, and efficient system.

REFERENCES

[1] C. M. Diez, A. Costabeber, F. Tardelli, D. Trainer, and J. Clare, "Control and experimental validation of the series bridge modular multilevel converter for hvdc applications," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2389–2401, 2019.

[2] M. Banaei, H. Ajdar Faeghi Bonab, and N. Taghizadegan Kalantari, "Analysis and design of a new single switch non-isolated buck-boost dc-dc converter," *J. Oper. Autom. Power Eng.*, vol. 8, no. 2, pp. 116–127, 2020.

[3] H. Yinghong, S. Peng, G. Qing, and C. Yu, "Capacitor voltage observation for series-connected-double submodule based modular multilevel converter," in *2022 4th International Conference on Power and Energy Technology (ICPET)*, pp. 276–281, IEEE, 2022.

[4] A. Saleki, S. Rezazade, B. J. Pordanjani, M. Gupta, and M. T. Bina, "A novel protective scheme to improve half-bridge mmc operation against dc fault condition," in *2022 13th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC)*, pp. 118–122, IEEE, 2022.

[5] Y. Song, Y. Luo, X. Xiong, F. Blaabjerg, and W. Wang, "An improved submodule topology of mmc with fault blocking capability based on reverse-blocking insulated gate bipolar transistor," *IEEE Trans. Power Delivery*, vol. 37, no. 3, pp. 1559–1568, 2021.

[6] A. Saleki, B. J. Pordanjani, and M. T. Bina, "Dc fault analysis in mmc based hvdc systems along with proposing a modified mmc protective topology for grid stability," in

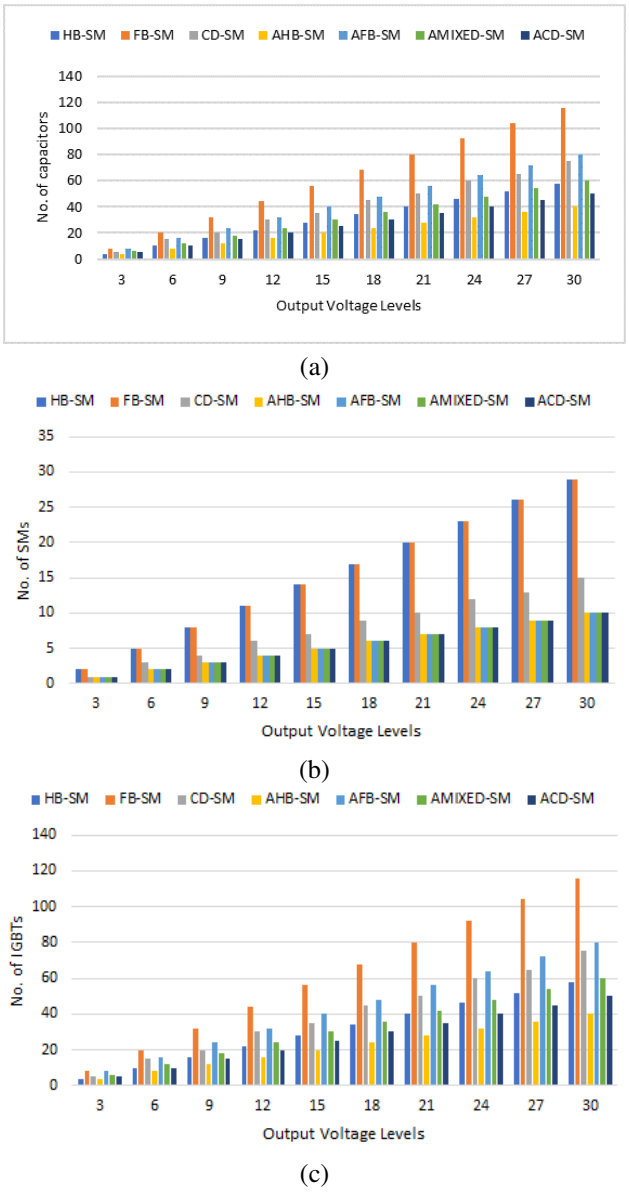


Fig. 10. Comparison of asymmetric CD-SM topology with other topologies (a) O/P voltage level Vs required number of capacitors, (b) O/P voltage level Vs required number of SMs, (c)) O/P voltage level V_s required number of IGBTs.

2021 25th Electrical Power Distribution Conference (EPDC), pp. 55–59, IEEE, 2021.

[7] U. Farooq and R. B. Bass, "Frequency event detection and mitigation in power systems: A systematic literature review," *IEEE Access*, vol. 10, pp. 61494–61519, 2022.

[8] J. Prommetta, J. Schindler, J. Jaeger, T. Keil, C. Butterer, and G. Ebner, "Protection coordination of ac/dc intersystem faults in hybrid transmission grids," *IEEE Trans. Power Delivery*, vol. 35, no. 6, pp. 2896–2904, 2020.

[9] Q. Yang and M. Saeedifard, "Analysis of the modular multilevel converter under single open-circuit fault in the upper active switch of a submodule," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1817–1824, IEEE, 2019.

[10] J. V. M. Farias, A. F. Cupertino, H. A. Pereira, S. I. Seleme, and R. Teodorescu, "On converter fault tolerance in mmc-hvdc systems: A comprehensive survey," *IEEE J. Emerging Sel. Top. Power Electron.*, vol. 9, no. 6, pp. 7459–7470, 2020.

[11] J. He, Q. Yang, and Z. Wang, "On-line fault diagnosis and fault-tolerant operation of modular multilevel converters—a comprehensive review," *CES Tras. Electr. Mach. Syst.*, vol. 4, no. 4, pp. 360–372, 2020.

[12] D. Che, J. Z. Bird, A. Hagmüller, and M. E. Hossain, "An adjustable stiffness torsional magnetic spring with a linear stroke length," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 5944–5948, IEEE, 2021.

[13] X. Yang, Y. Xue, B. Chen, Z. Lin, T. Q. Zheng, and Y. Li, "Novel modular multilevel converter against dc faults for hvdc applications," *CSEE J. Power Energy Syst.*, vol. 3, no. 2, pp. 140–149, 2017.

[14] X. Li, Q. Song, W. Liu, H. Rao, S. Xu, and L. Li, "Protection of nonpermanent faults on dc overhead lines in mmc-based hvdc systems," *IEEE Trans. Power Delivery*, vol. 28, no. 1, pp. 483–490, 2012.

[15] X. Hu, Y. Zhu, J. Zhang, F. Deng, and Z. Chen, "Unipolar double-star submodule for modular multilevel converter with dc fault blocking capability," *IEEE Access*, vol. 7, pp. 136094–136105, 2019.

[16] G. Tang, Z. Xu, and Y. Zhou, "Impacts of three mmc-hvdc configurations on ac system stability under dc line faults," *IEEE Trans. Power Syst.*, vol. 29, no. 6, pp. 3030–3040, 2014.

[17] K. V. Iyer, A. K. Sahoo, and N. Mohan, "Asymmetrical modular mutilevel converter (a-mmc) based hvdc system," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 4693–4699, IEEE, 2015.

[18] E. Seifi Najmi, A. Ajami, and A. Rajaei, "A generalized modular multilevel current source inverter," *J. Oper. Autom. Power Eng.*, vol. 5, no. 2, pp. 181–190, 2017.

[19] M. Hosseinpour, S. Mansoori, and H. Shayeghi, "Selective harmonics elimination technique in cascaded h-bridge multi-level inverters using the salp swarm optimization algorithm," *J. Oper. Autom. Power Eng.*, vol. 8, no. 1, pp. 32–42, 2020.

[20] K. Srivastav, A. K. Sahoo, K. V. Iyer, and N. Mohan, "Modulation, control, and performance analysis of asymmetric modular multilevel converter (a-mmc)," *IET Power Electron.*, vol. 11, no. 5, pp. 834–843, 2018.

[21] M. Rahimian, M. Hosseinpour, and A. Dejamkhooy, "A modified phase-shifted pulse width modulation to extend linear operation of hybrid modular multi-level converter," *J. Oper. Autom. Power Eng.*, vol. 6, no. 2, pp. 183–192, 2018.

[22] H. Liu, C. Zhang, L. Xu, X. Sun, S. Gu, and X. Li, "Voltage balancing control strategy for mmc based on nlm algorithm," in *2019 14th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, pp. 1075–1079, IEEE, 2019.

[23] J. Zeng, W. Lin, and J. Liu, "Switched-capacitor-based active-neutral-point-clamped seven-level inverter with natural balance and boost ability," *IEEE Access*, vol. 7, pp. 126889–126896, 2019.

[24] S. S. Lee, C. S. Lim, Y. P. Siwakoti, and K.-B. Lee, "Hybrid 7-level boost active-neutral-point-clamped (h-7l-banpc) inverter," *IEEE Trans. Circuits Syst. II: Express Briefs (Early Access)*, vol. 67, no. 10, pp. 2044–2048, 2019.

[25] G. Guo, H. Wang, Q. Song, J. Zhang, T. Wang, B. Ren, and Z. Wang, "Hb and fb mmc based onshore converter in series-connected offshore wind farm," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2646–2658, 2019.

[26] R. Marquardt, "Modular multilevel converter: An universal concept for hvdc-networks and extended dc-bus-applications," in *The 2010 International Power Electronics Conference-ECCE ASIA-*, pp. 502–507, IEEE, 2010.

[27] H. N. Chaudhari and P. B. Darji, "Asymmetrical modular multilevel converter (a-mmc) with mixed cell sub-modules (sm) for improved dc fault blocking capability and reduced component count," *Majlesi J. Electr. Eng.*, vol. 17, no. 1, pp. 63–74, 2023.