Journal of Operation and Automation in Power Engineering

Vol. 11, No. 4, Dec. 2023, Pages: 268-276

http://joape.uma.ac.ir

# A New Single-Phase Single-Stage Boost Inverter for Photovoltaic Applications

*P. Pakbaz, A. Nahavandi**

*Department of Electrical Engineering, Faculty of Engineering, Malayer University, Malayer, Iran*

***Abstract***— *In this paper a new single-phase single-stage high step up boost inverter appropriate for photovoltaic systems is proposed. In the proposed inverter, the duty cycle of one of the switches is adjusted to control the output voltage and increase the gain. In this structure, the dynamic model is adopted as an appropriate model to describe the low-frequency behaviour of converters and extracting the equations. Moreover, in this topology, a common ground is used between the input and output which can remove leakage current in different applications, including grid-connected applications. The proposed inverter is simulated using MATLAB/SIMULINK, and the experimental results are presented to verify the theoretical analysis.*

***Keywords***—Single-stage boost inverter, DC-AC converter, Renewable energy sources, Dynamic model.

## 1. INTRODUCTION

In recent years, due to the depletion of fossil fuels and global warming issues, the tendency to use distributed generation sources including wind turbines, photovoltaic power plants, small hydroelectric systems and fuel cells has risen. Among different distributed generations, photovoltaic systems have gained considerable popularity [1, 2]. Inverters are a major component of distributed generation systems. Among various inverters, single-stage inverters have recently gained considerable research attention thanks to their complete operation in one stage compared with multi-stage power converters [1]. Transformerless inverters are widely used in photovoltaic distribution systems. Removing the transformer in grid-connected photovoltaic systems confers different advantages, including a reduction in size, cost, weight, increase in system efficiency and easier installation. However, by removing the transformer, galvanic isolation between the PV system and the grid no longer exists; therefore, leakage current appears due to parasitic ground capacitance [3]. In [4], a boost inverter without isolation is proposed in which two similar DC-DC boost converters are connected to a DC source and load is connected to the output of converters in the differential form. In each half of a cycle, the inverter produces a sinusoidal output with a 180° phase difference with the other one. In [5], a single-phase single-stage inverter is presented to extract maximum power from the photovoltaic system according to the modification of a common two-stage full-bridge inverter. The new structure can operate as a buck-boost. In [6], a DC-AC converter is combined with a DC-DC converter as a single-stage structure. However, this structure has relatively low-efficiency due to leakage inductance. In [7], according to [5] and [6], a single-stage boost inverter is proposed that has high voltage gain compared with common two-stage structures. This structure uses an inductor with the capability of turn change to achieve high output voltage and allows it to operate at a low-input voltage. In addition, voltage gain can be adjusted by controlling the number of turns of the coupled inductor. The maximum efficiency of this structure is 89.3%. In [8] five-level single stage active neutral-point-clamped (ANPC) boost inverter is proposed. The proposed topology inherits high-frequency common mode voltage (CMV) mitigation ability as in the conventional ANPC inverter while gaining additional advantages such as voltage-boosting capability and enhanced dc-link voltage utilization. But the proposed inverter has large number of switches that leads to more power loss. In [9] two types of buck-boost inverter are proposed which have high reliability but in the proposed inverters several number of inductors are used that leads to high weight, size and power loss. In [10] an improved PWM method for achieving continuous input current in transformerless common ground boost inverter is presented. In [11] an isolated boost inverter is presented that has bidirectional power flow capability. The proposed inverter because of using of transformer is bulky and has high power loss. In [12] a single-stage buck-boost inverter for PV to grid connection is proposed that can track the maximum power point. Disadvantage of the proposed inverter is using of large number of switches. In [13, 14] a new transformerless inverter for reducing leakage current is proposed but it doesn't have boosting feature.

In [15], a new structure with a higher voltage gain compared with common inverters is presented. In this structure, all of the inductors are coupled, which leads to more compression and lower size.

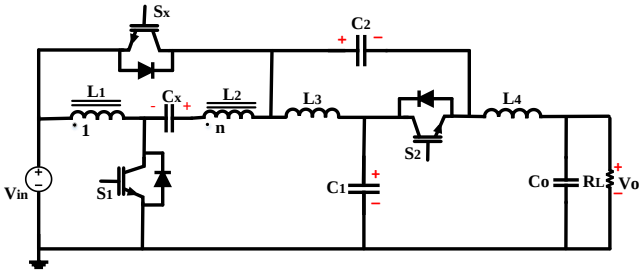



Fig. 1. Structure of the proposed inverter in Ref. [15]

Received: 19 Nov. 2021
Revised: 22 Jul. 2022
Accepted: 14 Aug. 2022
*Corresponding author:
E-mail: ali.nahavandi@malayeru.ac.ir (A. Nahavandi)
DOI: 10.22098/joape.2024.9865.1689
***Research Paper***

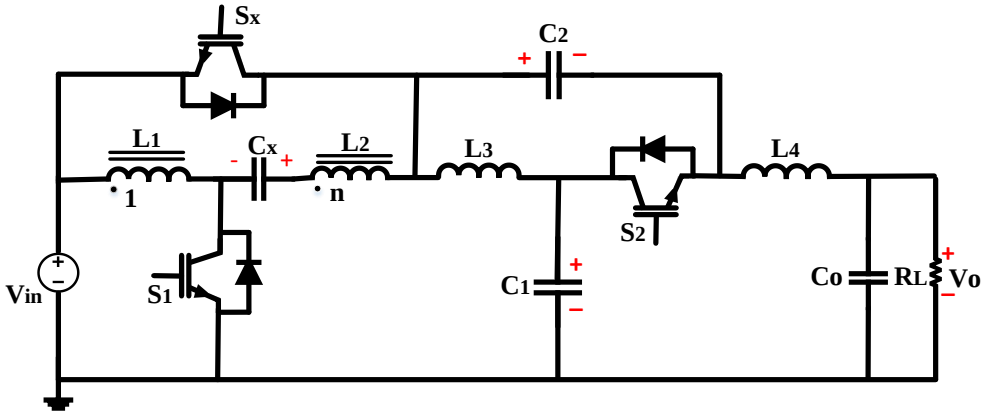



Fig. 2. Structure of the proposed inverter

Table 1. Switching model of the proposed inverter in a switching cycle

| | $S_1$ | $S_2$ | $S_3$ |
|---|---|---|---|
| Mode 1 | ON | OFF | ON |
| Mode 2 | ON | ON | OFF |
| Mode 3 | OFF | OFF | ON |
| Mode 4 | OFF | ON | OFF |

Adding a coupled inductor will increase voltage gain. The maximum efficiency of this structure is 90.5%. In [16], a single-phase single-stage buck-boost inverter is proposed. The dynamic model is used to extract equations. For this structure, maximum efficiency at the rated load and with a 100V input voltage is 95.7%. A review of the studies conducted in [4–7] shows that there is no common ground between the input and output. It is worth noting that structures proposed in [15, 16] have a common ground to remove leakage current. In [7, 15], a coupled inductor is used to regulate voltage and increase gain; however, this reduces efficiency due to the high value of leakage inductance of the coupled inductor.

In this paper, a single-phase boost inverter without isolation is proposed which shares a common terminal between input and output ports to remove leakage current. The proposed structure has three active switches and the output voltage can be regulated by duty cycle of one of the switches.

## 2. Operation Principles of the Proposed Inverter

This structure is proposed based on [15] displayed in Fig. 1. Fig. 2 depicts the structure of the proposed inverter which includes three IGBT switches, three inductors, and four capacitors. By comparing [15] and the proposed structure, it can be concluded that both have the same number of switches and capacitors; still, the coupled inductor in [15] is replaced with an inductor in the proposed structure which reduces the size and cost and increases efficiency due to the lack of leakage inductance. The proposed structure has the capability of output voltage regulation by adjusting the duty cycle of switch $S_1$ which allows operation at low-input voltages. The proposed inverter can generate AC voltage in a wide range. Moreover, this structure shares a common ground between $V_{in}$ and $V_o$ which can remove the effects of leakage current.

## 3. Modulation of the Proposed Inverter

Switch $S_1$operates by using PWM at a frequency of 10 KHz; however, to generate switching signals for $S_2$ and $S_3$, a sinusoidal pulse width modulation (SPWM) is employed (Fig. 3). To produce

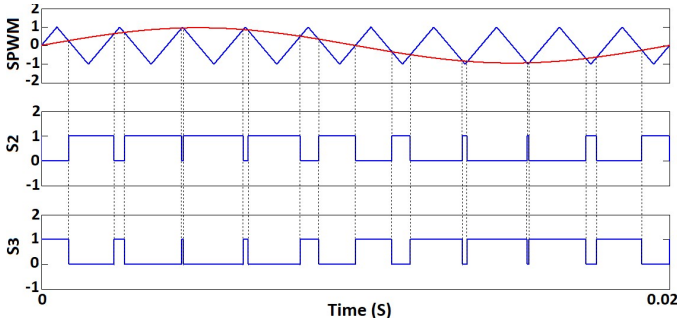



Fig. 3. SPWM of the proposed inverter

signals, a sinusoidal waveform with the frequency of 50Hz which determines the output voltage frequency, and a triangle wave with the frequency of 20 KHz which determines switching frequency is compared. If the sinusoidal wave is more than the triangle wave, switch $S_2$ is on; otherwise, switch $S_3$ is on. The operation of the proposed inverter over a switching cycle '$T_S$' is depicted in Fig 4. To avoid complicated modes analysis, the conduction time of $S_1$ and $S_2$ is tuned to half of the switching cycle $T_{S1}$ and $T_{S2}$, respectively.

## 4. Analysis of Operation Modes of the Proposed Inverter

The switching frequency of $S_1$ and $S_2$ is 10 KHz and 20 KHz, respectively. In general, as listed in Table**??**, four operation modes occur. Therefore, the proposed inverter has four operation modes in each half-cycle.

### 4.1. Mode 1 ($t_0$-$t_1$)

In this mode, switches $S_1$ and $S_3$ are on and switch $S_2$ is off (Fig. 5(a)). Inductor $L_1$ is charged by the input DC source through switch $S_1$. The energy stored in inductor $L_2$ and $C_1$ and $C_3$ capacitors is transferred to the output through switch $S_3$. Note that inductor $L_2$ is discharged to zero. Equations of this mode can be derived as:

$$v_{L_1} = v_{in} \tag{1}$$

$$v_{L_2} = v_{C_1} - v_{C_3} \tag{2}$$

$$v_{L_3} = v_{C_3} - v_{C4} \tag{3}$$

$$i_{c_1} = i_{L_2} \tag{4}$$

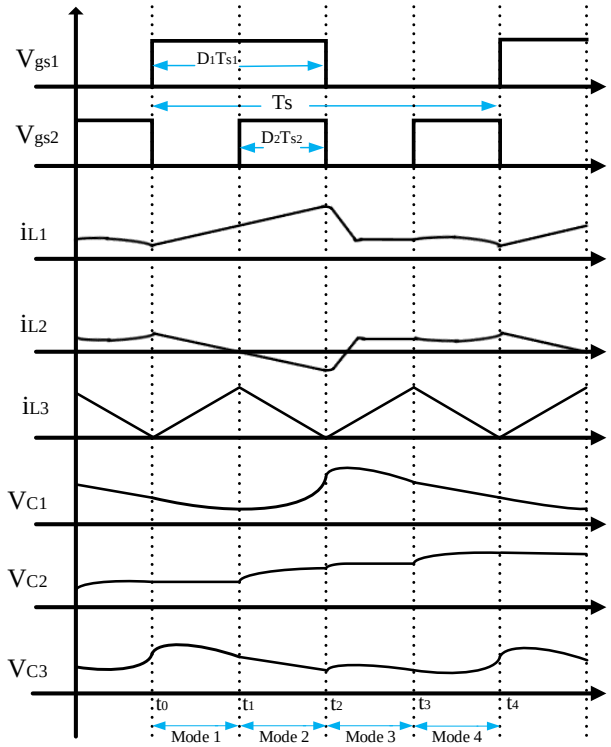



Fig. 4. Waveform of the proposed inverter

$$i_{c_2} = 0 \tag{5}$$

$$i_{c_3} = i_{L_3} - i_{L_2} \tag{6}$$

$$i_{c_4} = i_{L_3} - i_O \tag{7}$$

### 4.2. Mode 2 ($t_1$-$t_2$)

Here, switches $S_1$ and $S_2$ are on and switch $S_3$ is off (Fig. 5(b)). Inductor $L_1$ is still being charged by the input source. At the beginning of this mode, inductor $L_3$ and the capacitor $C_3$ were charged. According to the continuity of the current in the inductor, the energy stored in $L_3$ and $C_3$ through reverse parallel diode of $S_2$ and $L_2$ is transferred to $C_1$, $C_2$ and the output. Equations of this mode can be derived as:

$$v_{L_1} = v_{in} \tag{8}$$

$$v_{L_2} = v_{C_1} - v_{C_3} \tag{9}$$

$$v_{L_3} = -v_{C_2} - v_{C_4} \tag{10}$$

$$i_{c_1} = -i_{L_2} \tag{11}$$

$$i_{c_2} = i_{L_3} \tag{12}$$

$$i_{c_3} = -i_{L_2} \tag{13}$$

$$i_{c_4} = i_{L_3} - i_O \tag{14}$$

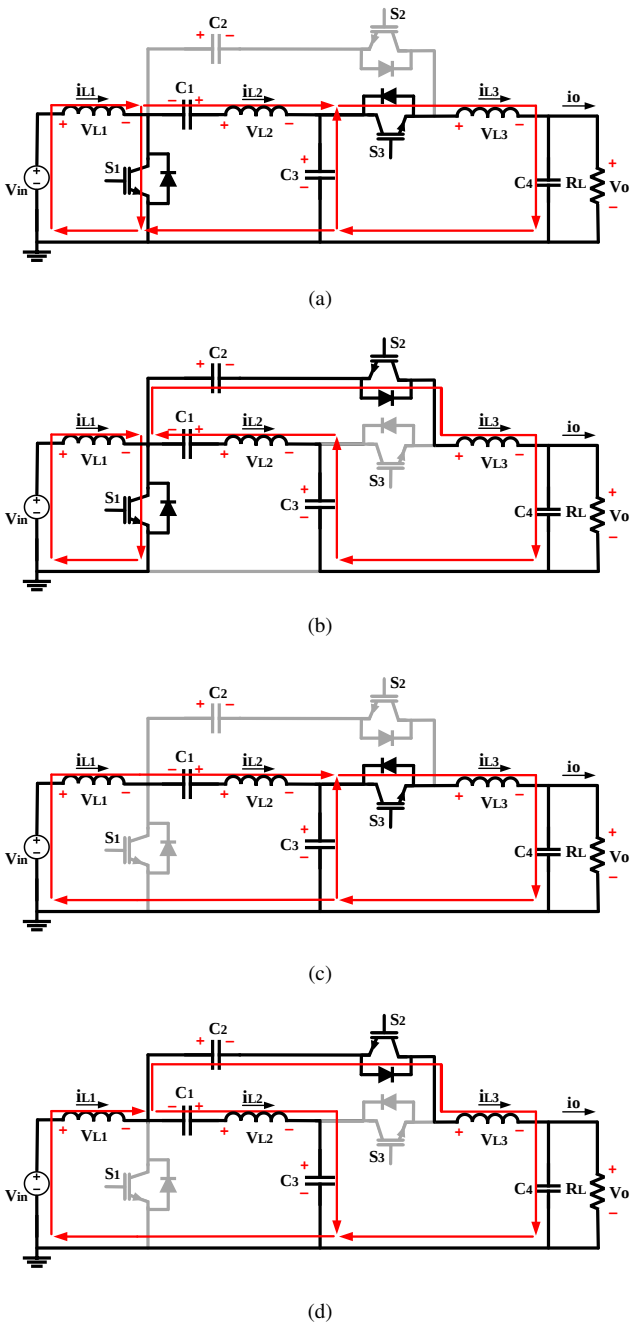



Fig. 5. Operation modes of the proposed inverter in a switching cycle '$T_S$' (a) mode 1,(b)mode 2, (c) mode 3 and (d) mode 4

### 4.3. Mode 3: ($t_2$-$t_3$)

In this mode, switches $S_1$ and $S_2$ are turned off and switch $S_3$ is turned on (Fig. 5(c)). There is a transient state at the beginning of this mode. The energy stored in $L_1$and $L_2$ is transferred to capacitor $C_2$ and the output through reverse parallel diode $S_2$. Since switch $S_3$ is turned on in this mode, the voltage of capacitor $C_3$ applies to the cathode of the reverse parallel diode $S_2$, and then diode turns off. In the following, the energy stored in $L_1$ and $C_1$ is transferred to the output through switch $S_3$ and $L_2$. Moreover, the energy stored in $C_3$ is transferred to the output through switch $S_3$. Equations of this mode can be derived as:

$$v_{L_1} = v_{in} - \frac{v_{in}}{1 - D_1} \tag{15}$$

$$v_{L_2} = \frac{v_{in}}{1-D_1} + v_{C_1} - v_{C_3} \tag{16}$$

$$v_{L_3} = v_{C_3} - v_{C_4} \tag{17}$$

$$i_{c_1} = (1-D_1)\, i_{in} \tag{18}$$

$$i_{c_2} = 0 \tag{19}$$

$$i_{c_3} = i_{L_3} - (1-D_1)\, i_{in} \tag{20}$$

$$i_{c_4} = i_{L_3} - i_o \tag{21}$$

### 4.4. Mode 4: ($t_3$-$t_4$)

During this mode, switches $S_1$ and $S_3$ are turned off and the reverse parallel diode of $S_2$ conducts (Fig. 5(d)). Therefore, energy from the source is transferred to $C_2$ and the output through reverse parallel diode of $S_2$. Also, the energy stored in $C_1$ is transferred to $C_3$ through $L_2$. Equations of this mode can be derived as:

$$v_{L_1} = v_{in} - \frac{v_{in}}{1-D_1} \tag{22}$$

$$v_{L_2} = \frac{v_{in}}{1-D_1} + v_{C_1} - v_{C_3} \tag{23}$$

$$v_{L_3} = \frac{v_{in}}{1-D_1} - v_{C_2} - v_{C_4} \tag{24}$$

$$i_{c_1} = (1-D_1)\, i_{in} - i_{L_3} \tag{25}$$

$$i_{c_2} = (1-D_1)\, i_{in} - i_{L_2} \tag{26}$$

$$i_{c_3} = (1-D_1)\, i_{in} - i_{L_3} \tag{27}$$

$$i_{c_4} = i_{L_3} - i_O \tag{28}$$

## 5. OBTAINING OF VOLTAGE STATIC GAIN

The large signal matrix averaged model $\overline{A}_I$ of the proposed converter in terms of duty cycles $D_1$, $D_2$ and $D_2{}'$ is obtained as follows for four operation modes.

$$\overline{A}_{\mathrm{I}} = \frac{d}{dt}\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ i_{L_3} \\ v_{C_1} \\ v_{C_2} \\ v_{C_3} \\ v_{C_4} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{2}{L_2} & 0 & -\frac{2}{L_2} & 0 \\ 0 & 0 & 0 & 0 & -\frac{2D_2}{L_3} & \frac{2D_2'}{L_3} & -\frac{2}{L_3} \\ \frac{(1-D_1)}{C_1} & \frac{(D_2'-D_2)}{C_1} & -\frac{D_2}{C_1} & 0 & 0 & 0 & 0 \\ \frac{D_2(1-D_1)}{C_2} & -\frac{D_2}{C_2} & \frac{D_2}{C_2} & 0 & 0 & 0 & 0 \\ \frac{(1-D_1)(D_2-D_2')}{C_3} & -\frac{D_2+D_2'}{C_3} & \frac{(2D_2'-D_2)}{C_3} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_4} & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ i_{L_3} \\ v_{C_1} \\ v_{C_2} \\ v_{C_3} \\ v_{C_4} \end{bmatrix} + \begin{bmatrix} \frac{(1-2D_1)}{(1-D_1)L_1} \\ \frac{1}{(1-D_1)L_2} \\ \frac{D_2}{(1-D_1)L_3} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ -\frac{1}{C_4} \end{bmatrix} i_O$$

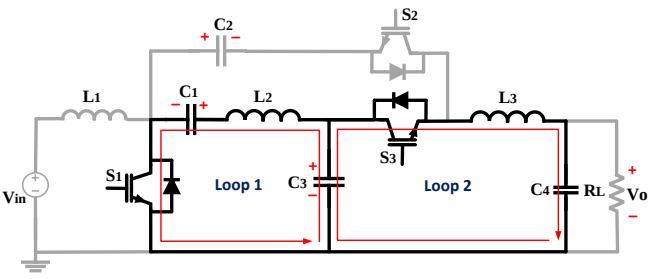



Fig. 6. Resonance loops

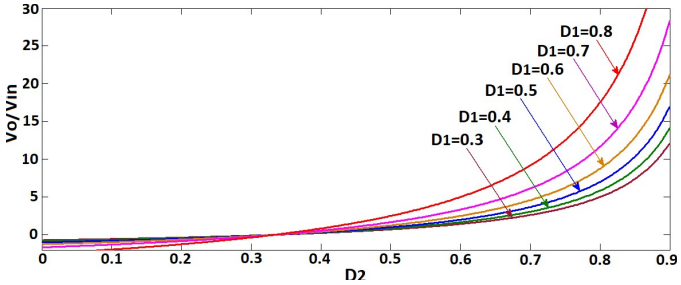



Fig. 7. Voltage gain in terms of $D_2$ for different values of $D_1$

where $D_2 = 1 - D_2'$, $i_L$ is the instantaneous current flowing though the inductors, and $v_C$ is the instantaneous voltage of the capacitors. By applying the volt-second balance law to inductors and the charge-second balance to capacitors in four modes, the gain will be obtained:

$$(1-D_1)\, i_{L_1} + (1-2D_2)\, i_{L_2} - D_2 i_{L_3} = 0 \tag{29}$$

$$D_2\,(1-D_1)\, i_{L_1} - D_2 i_{L_2} + D_2 i_{L_3} = 0 \tag{30}$$

$$(1-D_1)\,(2D_2-1)\, i_{L_1} - i_{L_2} + (2-3D_2)\, i_{L_3} = 0 \tag{31}$$

$$i_{L_3} = i_O \tag{32}$$

Table 2. Comparison between the proposed inverter and [7, 15] and [16]

| parameters | Ref. [7] | Ref. [15] | Ref. [16] | Proposed Inverter |
|---|---|---|---|---|
| Input Voltage($V_{in}$) | 35-48 | 62 | 60-100 | 58 |
| Number of switches | 4 | 3 | 4 | 3 |
| Number of Inductors | 1 | 2 | 2 | 3 |
| Number of capacitors | 2 | 4 | 3 | 4 |
| Number of Diodes | 3 | 0 | 0 | 0 |
| Number of Coupled Inductors | 1 | 1 | 0 | 0 |
| Switching frequency | 50KHz | 20KHz | 50KHz | $S_1$=10KHz, $S_{2,3}$=20KHz |
| $V_O$ (rms) | 110V | 110V | 110V | 110V |
| Voltage Gain | $\frac{1+nD}{1-D}$ | $\frac{(2n+3)(2D-1)+1}{2D}$ | $\frac{D}{1-D}$ | $\frac{3D_2-1}{2(1-D_1)(1-D_2)}$ |
| Output Power | 200W | 280W | 300W | 287W |
| Efficiency | 89.3% | 90.5% | 95.7% | 98.3% |
| Input Current | Discontinuous | Quasi-Continuous | Continuous | Continuous |
| Voltage Stress of Switches | $M_1$=340V<br>$M_2$=340V<br>$M_3$=340V<br>$M_4$=340V | $S_1$=220V<br>$S_2$=440V<br>$S_x$=440V | $S_1$=200V<br>$S_2$=200V<br>$S_3$=200V<br>$S_4$=200V | $S_1$=110V<br>$S_2$=110V<br>$S_3$=72V |

Table 3. Parameters of the proposed inverter in simulation

| Parameter | Parameter |
|---|---|
| Input voltage | 12V |
| $C_1$=$C_3$=$C_4$ | 100F |
| $C_2$ | 200 F |
| $L_1$ | 200H |
| $L_2$=$L_3$ | 300H |
| Switching frequency of $S_1$ | 10KHz |
| Switching frequency of $S_2$=$S_3$ | 20KHz |

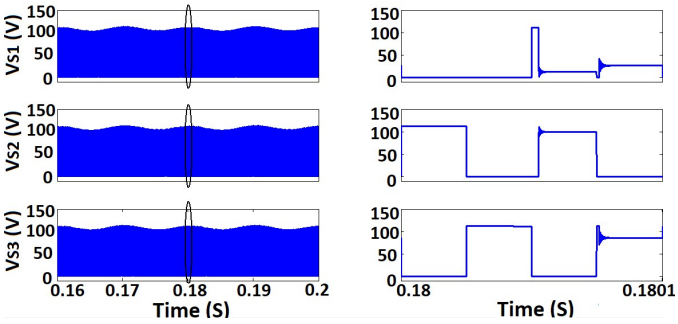



Fig. 10. Voltage stress waveform of the switches

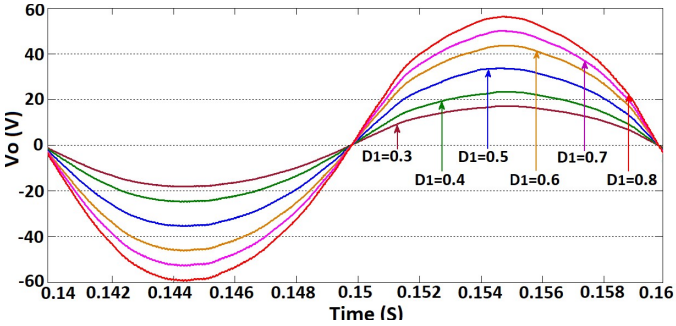



Fig. 8. Output voltage based on adjusting $D_1$

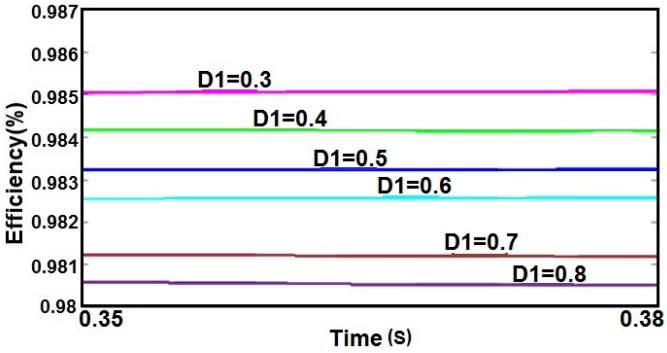



Fig. 11. Efficiency for different values of $D_1$ in the range of 0.3-0.8

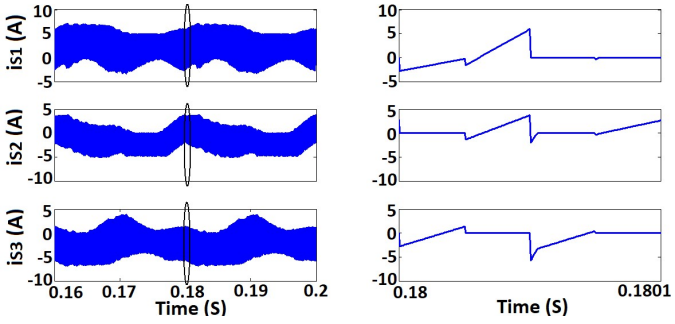



Fig. 9. Current stress waveform of the switches

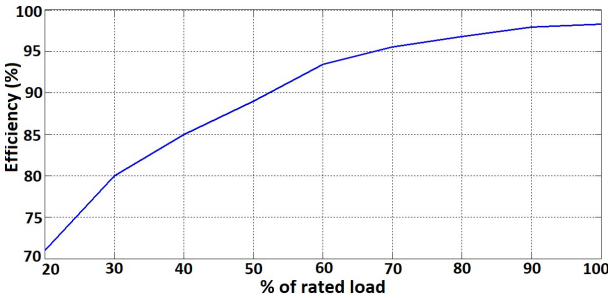



Fig. 12. Variations of efficiency in terms of different load conditions

Equation (30) can be summarized as follows:

$$i_{L_2} = (1 - D_1)\, i_{L_1} + i_{L_3} \tag{33}$$

By placing Equation (33) in Equation (29), Equation (34) is obtained as follows:

$$2\,(1 - D_1)\,(1 - D_2)\, i_{L_1} = (3D_2 - 1)\, i_{L_3} \tag{34}$$

By placing Equation (32) in Equation (34), the following equation is obtained:

$$2\,(1 - D_1)\,(1 - D_2)\, i_{L_1} = (3D_2 - 1)\, i_O \tag{35}$$

Based on Equation (35) and considering $i_{L1}$=$i_{in}$, the static current gain is calculated as follows:

$$\frac{i_O}{i_{in}} = \frac{2\,(1 - D_1)\,(1 - D_2)}{3D_2 - 1} \tag{36}$$

Since the gain of current and voltage are the reverse of each other, voltage gain can be calculated as Equation (37).

$$\frac{v_O}{v_{in}} = \frac{3D_2 - 1}{2\,(1 - D_1)\,(1 - D_2)} \tag{37}$$

Furthermore, according to current of switches in each mode, the current stress on switches can be written as follows.

$$i_{S_1} = \frac{-4D_1D_2^2 + D_1D_2 + 4D_2^2 + D_1 + 2D_2 - 2}{2\,(1 - D_1)\,(1 - D_2)} i_O \tag{38}$$

$$i_{S_2} = -2D_2 i_O \tag{39}$$

$$i_{S_3} = 2D_2{}' i_O \tag{40}$$

## 6. Resonance Mode Analysis

Two inductive and capacitive loops are shown in Fig. 6, and the resonance mode is analyzed for them. First, the resonance frequency is calculated for loop 1 as follows:

$$C_{eq} = \frac{C_1 \times C_3}{C_1 + C_3} = \frac{\left(100 \times 10^{-6}\right) \times \left(100 \times 10^{-6)}\right)}{100 \times 10^{-6} + 100 \times 10^{-6}} = 50{\times}10^{-6}\mu \tag{41}$$

$$f_{o_1} = \frac{1}{2\pi\sqrt{L_2 \times C_{eq}}} = \frac{1}{2\pi\sqrt{300 \times 10^{-6} \times 50 \times 10^{-6}}} = 1300Hz \tag{42}$$

It should be noted that the $C_1$=$C_4$and $L_2$=$L_3$, therefore resonance frequency of loop 1 and loop 2 equal to each other as equation (43).

$$f_o = f_{o_1} = f_{o_2} = 1300Hz \tag{43}$$

Since the frequency of switch $S_1$is $f_{S1}$=10 KHz and that of switch 2 is $f_{S2}$=20 KHz, the resonance mode has not occurred for the proposed inverter:

$$f_{s_2} = 20KHz > f_{s_1} = 10KHz > f_o = 1300Hz \tag{44}$$

## 7. Analysis of Components Desigining

There are following equation for voltage of inductor $L_1$:

$$v_{L_1} = L_1 \frac{di_{L_1}}{dt} \tag{45}$$

Which can be written as:

$$L_1 = \frac{D_1T_1}{\Delta i_{L_1}} v_{L_1} \tag{46}$$

Where ΔiL1 is inductor current ripple. The acceptable maximum inductor current ripple determines the minimum value of inductance.

$$L_{1\,\min} = \frac{D_{\max}T_1}{\Delta i_{L_{1\,\max}}} v_{in} \tag{47}$$

There are similar equations for other inductors.

Also, for capacitor $C_1$:

$$i_{C_1} = C_1 \frac{dv_{C_1}}{dt} \tag{48}$$

Which can be written as:

$$C_1 = \frac{D_2T_2}{\Delta v_{C_1}} i_{C_1} \tag{49}$$

Where $\Delta v_{c1}$ is capacitor voltage ripple. The acceptable maximum capacitor voltage ripple determines the minimum value of capacitance.

$$C_{1\,\min} = \frac{D_{\max}T_2}{\Delta v_{C_{1\,\max}}} i_{L_2} \tag{50}$$

On the other hand from equations (33), (34) and (35), following equation is obtained:

$$i_{L_2} = \left(\frac{3D_2 - 1}{2\,(1 - D_2)} + 1\right) i_O \tag{51}$$

Therefore by substituting (51) in (50):

$$C_{1\,\min} = \frac{D_{\max}T_2}{\Delta v_{C_{1\,\max}}} \times \left(\frac{3D_{\max} - 1}{2\,(1 - D_{\max})} + 1\right) i_O \tag{52}$$

There are similar equations for other capacitors:

$$C_{2\,\min} = \frac{D_{\max}T_2}{\Delta v_{C_{2\,\max}}} i_O \tag{53}$$

$$C_{3\,\min} = \frac{D_{\max}T_2}{\Delta v_{C_{3\,\max}}} i_O \tag{54}$$

$$C_{4\,\min} = \frac{D_{\max}T_2}{\Delta v_{C_{4\,\max}}} i_O \tag{55}$$

## 8. Comparison Between the Proposed Inverter and [7, 15] and [16]

In table **??** the proposed inverter is compared with the inverters which are proposed in reference [7, 15] and [16]. It is obvious that in same duty cycle the proposed inverter has more voltage gain than inverter proposed in [7, 15] and [16]. Also, the proposed inverter has more efficiency than inverter proposed in [7, 15] and [16].

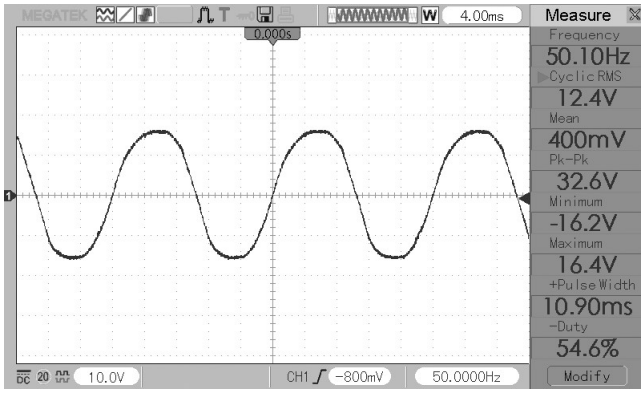
## 9. Simulation Results

To clarify the advantages of the proposed converter, in this paper, simulation is performed by MATLAB/Simulink software. In Table3 the simulation parameters of the proposed inverter are presented.

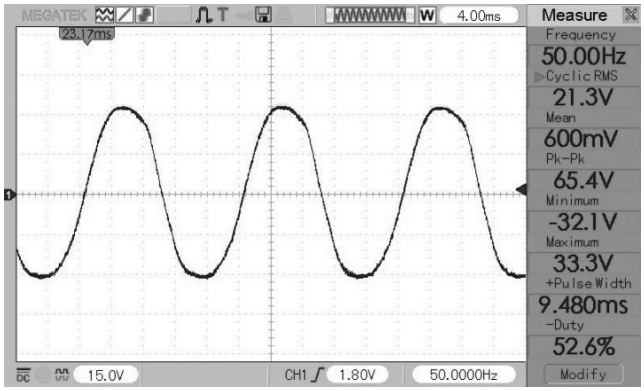
Note that by changing the value of $D_1$, the ratio of the output voltage to input voltage changes according to Equation (37). In Fig. 7 the voltage gain in terms of $D_2$ for different values of $D_1$ in the range of 0.3-0.8 is presented. In Fig. 8, the AC output voltage is presented when the input voltage is 12V DC. The output voltage is illustrated for different values of $D_1$ in the range of 0.3-0.8. Based on this figure, the output voltage significantly increases by raising of $D_1$.

In Fig. 9, the current stress waveform of the switches is shown. Fig. 10 also shows the voltage stress waveform of the switches.

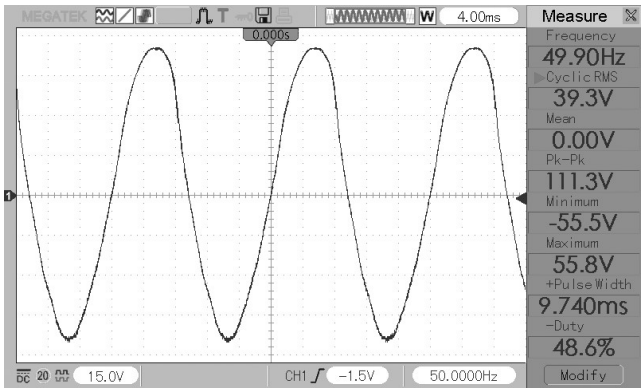
Fig. 11 displays efficiency for different value of $D_1$. Evidently, by increasing the duty cycle, efficiency drops. However, this reduction is negligible because by varying $D_1$ in the range of 0.3-0.8, efficiency decreases to less than 0.5%. In Fig. 12, the efficiency of the proposed inverter for different load conditions is depicted. By increasing the load, current drops, and by reducing the current, power loss in circuit elements is reduced and, consequently, efficiency is increased.




(a)




(b)




(c)

Fig. 13. Experimental waveforms (a) Output voltage with $D_1$=0.3, (b)Output voltage with $D_1$=0.5 and (c) Output voltage with $D_1$=0.8

## 10. Experimental Results

A prototype was built and tested to validate the performance of the proposed inverter. The same parameters were used as those in the simulation based on Table??. The BUP314D was employed as the power switches. Fig. 13 shows the experimental waveforms of the output voltages with $D_1$=0.3, $D_1$=0.5 and $D_1$=0.8. Clearly, by increasing the duty cycle of switch $S_1$, the output voltage increases.

In Figs. 14-16, diagrams are shown with $D_1$=0.5. In Fig. 14, the current of inductor $L_1$ is shown. The voltages across switches are presented ($v_{S1}$, $v_{S2}$, and $v_{S3}$) in Fig. 15. Fig. 16 shows the capacitors' voltages ($v_{C1}$, $v_{C2}$ and $v_{C3}$), and Fig. 17 illustrates the prototype of the proposed inverter.

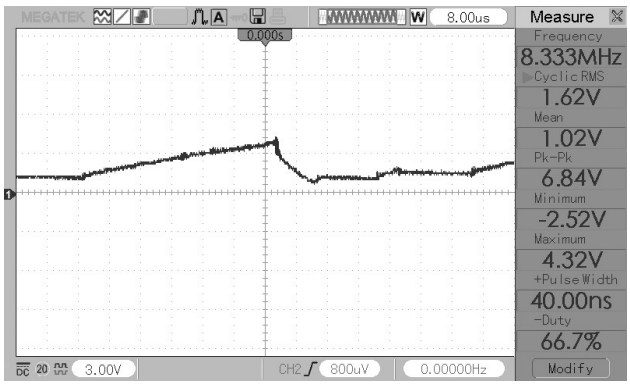
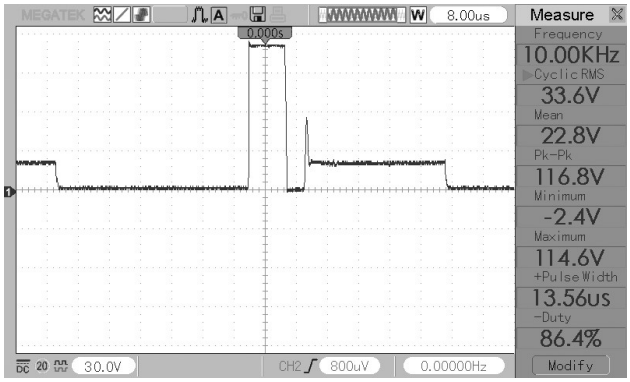
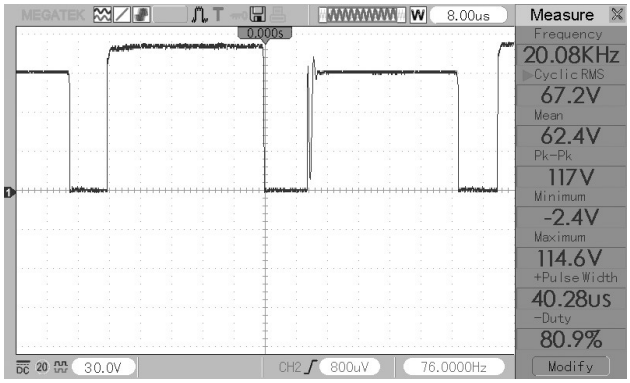


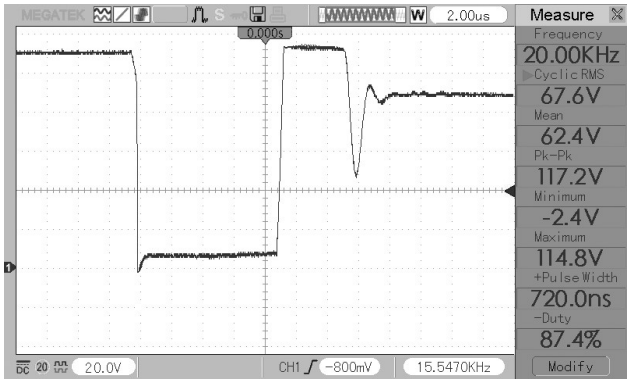

Fig. 14. Experimental waveforms of $i_{L1}$




(a)

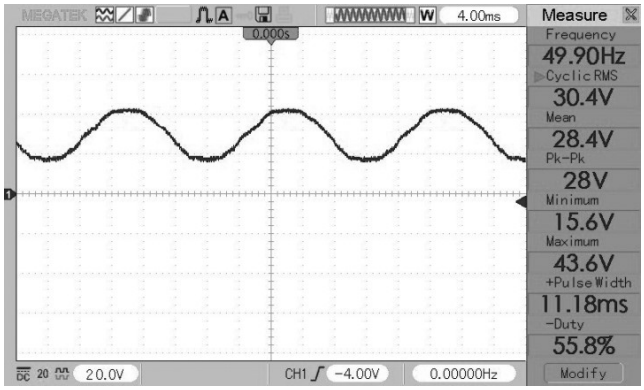



(b)

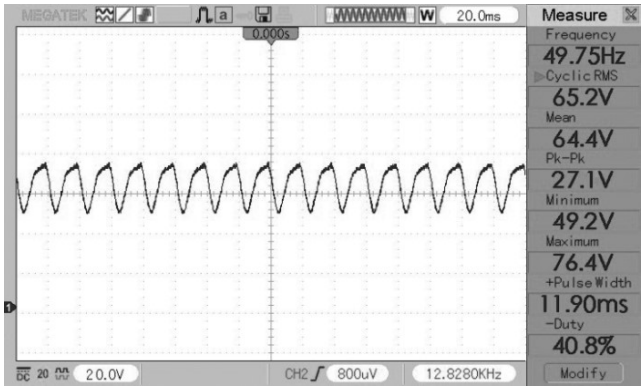



(c)

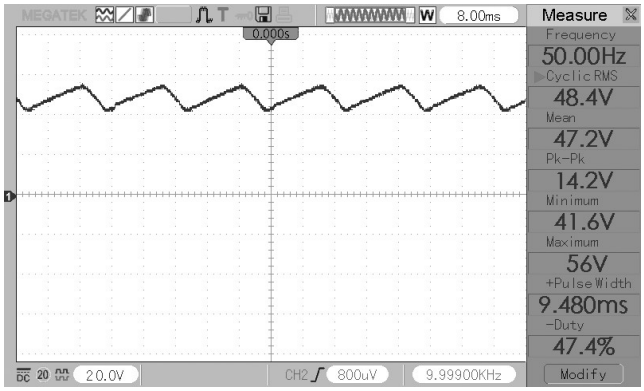
Fig. 15. Experimental waveforms of voltage stress on (a) $S_1$, (b) $S_2$ and (c) $S_3$




(a)




(b)

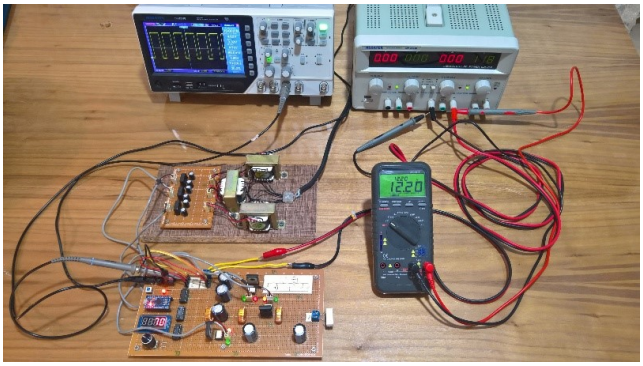



(c)

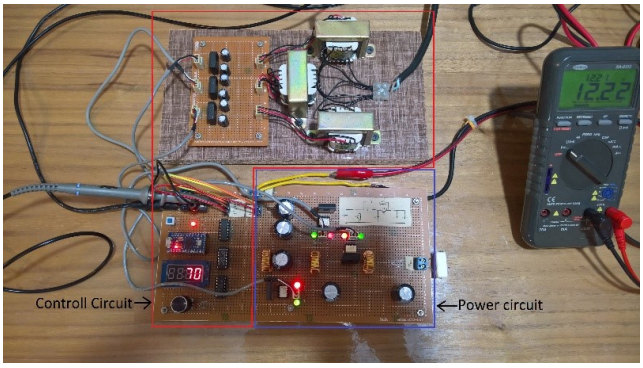
Fig. 16. Experimental waveforms (a) Voltage waveform of $C_1$, (b) Voltage waveform of $C_2$ and (c) Voltage waveform of $C_3$

## 11. CONCLUSION

In this paper, a single-phase single-stage step up inverter with three active switches has been presented. The operation principles of the proposed structure are investigated in four operation modes, and the large signal and the static gain are calculated. The proposed inverter shares a common ground between the input DC port and output AC port. Therefore, the ground leakage current problem, particularly in transformer-less grid-tied PV applications, can be eliminated. The proposed inverter has the advantage of high voltage step-up which can be further increased by adjusting the duty cycle of switch $S_1$. By adjusting the duty cycle, the inverter can control the output voltage. Simulation was performed in MATLAB/Simulink. An experimental prototype was built with an input voltage of 12V, which demonstrated the high efficiency of the inverter. The simulation and experimental results confirmed the operation of the proposed structure.



(a)




(b)

Fig. 17. Prototype photo of the proposed inverter

## REFERENCES

[1] Y. Zhou and W. Huang, "Single-Stage Boost Inverter with Coupled Inductor," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1885 – 1893, Apr. 2012.

[2] K. Y. Lo, Y. M. Chen and Y. R. Chang, "Bi-Directional Single-Stage Grid-Connected Inverter for Battery Energy Storage System," IEEE Trans. Ind. Electron., vol. 64, no. 6, pp. 4581 – 4590, Jun 2017.

[3] N. Vázquez,M. Rosas, C. Hernández, E. Vázquez and F. j. Perez-Pinal, "A New Common-Mode Transformerless Photovoltaic Inverter, " *IEEE Trans. Ind Electron.*, vol. 62, no. 10, pp. 6381 – 6391, Oct 2015.

[4] R. O. Caceres and I. Barbi, "A Boost DC–AC Converter: Analysis, Design, and Experimentation," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 134 – 141, Jan 1999.

[5] H. Ribeiro, F. Silva, S. Pinto and B. Borges, "Single stage inverter for PV applications with one cycle sampling technique in the MPPT algorithm," *Proc. 35$^t$h Annu. Conf. IEEE Ind. Electron.*,2009, pp. 842–849.

[6] H. Ribeiro, A. Pinto and B. Borges, "Single-stage DC-AC converter for photovoltaic systems," I*EEE Energy Convers. Congr. Expo.*,2010, pp. 604–610.

[7] A. Abramovitz, B. Zhao and K. Smedley, "High-Gain Single-Stage Boosting Inverter for Photovoltaic Applications," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3550 – 3558, May 2016.

[8] S. S. Lee, Y.Yang, Y. P. Siwakoti, " A Novel Single-Stage Five-Level Common-Ground Boost-Type Active Neutral-point-Clamped (5L-CGBT-ANPC) Inverter," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6192 – 6196, Jun 2021.

[9] A. A. Khan, Y. W. Lu, W. Eberle, L. Wang, U. A. Khan, H. Cha, " Single-phase Spilt-Inductor Differential Boost Inverters," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 107 – 120, Jan 2020.

[10] S. S. Lee, Y. P. Siwakoti, C. S. Lim, K. B. Lee, " An Improved PWM Technique to Achieve Continuous Input Current in Common-Ground Transformeless Boost Inverter," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 67, no. 12, pp. 3133 – 3136, Dec 2020.

[11] B. Ji, F. Hong, A. Shen, W. XV, C. Jiang, " An Isolated Single Stage Four-Quadrant Inverter with Energy Storage Capacitor," *IEEE Access*, vol. 9, , pp. 79643 – 79650, Mar 2021.

[12] K .K. M. Siu, C. N. Ho, "System Model and Performance Evaluation of Single-Stage Buck-Boost Type Manitoba Inverter for PV Applications," *IEEE J. Emerging Sel. Top. Power Electron.*, vol. 8,no. 4, pp. 3457 – 3466, Dec 2020.

[13] M.F Kangarlu, F. Mohammadi, "Performance Improvement of Single-Phase Transformer less Grid-Connected PV Inverters Regarding CMV and LVRT," *J. Oper. Autom. Power Eng.*, vol. 7, no. 1, pp. 1 – 15, May2019.

[14] F. Mohammadi, J. Milimonfared, H. Rastegar, M.F Kangarlu,, "Design of Single-Phase Transformerless Grid-Connected PV Inverter Considering Reduced Leakage Current and LVRT Grid Codes," *J. Oper. Automa. Power Eng.*, vol. 9, no. 1, , pp. 49 – 59, Apr 2021.

[15] K. Kim, H. Cha and H. G. Kim, "A New Single-Phase Switched-Coupled-Inductor DC-AC Inverter for Photovoltaic Systems," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5016 – 5022, Jul 2017.

[16] A. Kumar and P. Sensarma, "A Four-Switch Single-Stage Single-Phase Buck–Boost Inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5282 – 5292, Jul 2017.

[17] R. W. Erickson and D. Maksimovic, "Fundamentals of Power Electronics," *Kluwer Academic Publishers*, 2011.

[18] Y. Zhou, W. Huang, P. Zhao, J. Zhao, "Coupled-inductor single-stage boost inverter for grid-connected photovoltaic system," *IET Power Electron.*, vol. 7, no. 2, pp. 259 – 270, Feb 2014.

[19] T. Sreekanth, N. Lakshminarasamma and M. K. Mishra, "A Single Stage Grid Connected High Gain Buck-Boost Inverter with Maximum Power Point Tracking," *IEEE Trans. Energy Convers.*, vol. 32, no. 1, pp. 330 – 339, Mar 2017.

[20] Y. Zhou,W. Huang,F. Hong, Ch. Wang"Modelling analysis and power loss of coupled-inductor single-stage boost inverter based grid-connected photovoltaic power system," *IET Power Electron.*, vol. 9, no. 8, pp. 1664 – 1674, Jun 2016.

[21] A. K. Kaviani and B. Mirafzal, "A Switching Pattern for Single-Phase Single-Stage Current-Source Boost-Inverter," 27th Annu. *IEEE Applied Power Electron.*, Conf. & Expo, pp. 2066-2071, 2012.

[22] H. H. Shin, H. Cha, H. Kim and H. G. Kim, "Extended Boost Single-phase qZ-Source Inverter for Photovoltaic Systems," *J. Power Electron.*, vol. 14, No. 5, pp. 918-925, Sept 2014.

[23] T. Sreekanth,N. Lakshminarasamma, M. K. Mishra"Coupled inductor-based single-stage high gain DC–AC buck–boost inverter," *IET Power Electron.*, vol. 9, no. 8, pp. 1590 – 1599, Jun 2016.

[24] M. Kh. Nguyen, T. T. Tran"A Single-Phase Single-Stage Switched-Boost Inverter with Four Switches," *IEEE Trans. Power Electron.*, Vol. 33, No. 8, pp. 6769 – 6781, Aug. 2018.

[25] K. Y. Lo, Y. M. Chen, Y. R. Chang, "Bi-Directional Single-Stage Grid-Connected Inverter for Battery Energy Storage System," *IEEE Trans. Ind. Electron.*, vol. 64, No. 6, pp. 4581 – 4590, Jun 2017.

[26] J. Kan, S. Xie, Y. Wu, Y. Tang, Zh. Yao and R. Chen, "Single-Stage and Boost-Voltage Grid-Connected Inverter for Fuel-Cell Generation System," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5480 – 5490, Sept. 2015.

[27] Y. Shi, Z. Pan, R. Rodrigues, Ch. Wei, "A low-cost single-stage PV inverter," *IEEE Power Electron., Conf. Expo.*, pp. 2470-6647, Mar 2018.