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A New Transformerless DC-DC Converter for Renewable Energy Applications

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Abstract- *In this paper, a novel high step-up voltage switching cell formed by four passive elements and three diodes is proposed. The proposed cell can be integrated into a family of boost converters to obtain substantial dc gain as required by an electrical grid supplied such as solar or fuel cell. It is integrated into a boost converter; a new converter is obtained. The features of a new converter are significant dc gain without extreme duty cycle which enables the use of lower voltage and R_{Ds-on} MOSFET switch so as to reduce cost, the low-stress voltage on the switch and diodes, non-pulsating input current, easiness design and operation, single switch which means easiness of transistor driving, and line-load common ground. In addition, the low-voltage stress across diode allows using Schottky rectifiers to eliminate the reverse recovery current which leads to more reduction in conduction and switching losses. The equations of voltage and current in "continuous conduction mode (CCM) and discontinuous mode (DCM)" are extracted. Moreover, the voltage and current stresses on elements and switch are calculated. Finally, the performance of the proposed converter is validated by simulation results and experimental results to confirm theoretical calculation.*

Keyword—High step up dc gain, Low voltage stress, A new step up switching cell, Single switch.

1. INTRODUCTION

IN recent years, many applications are needed high step-up DC-DC converters such as medical equipment, servo motor drives, industrial applications, portable devices(e.g. portable computer and mobile phones), internet services and Renewable Energy Sources(RES) (e.g. solar cell, fuel cell and wind generation). One of the most critical issues of using RES is variable output energy and low output voltage due to depending on sunlight [1, 2].
In order to avoid this limitation, steep high dc-dc converters have been used. However, the simple structure and control, accessible design and operation analysis, and high gain ratio are the remaining challenges of dc-dc converters [3]. Also, the voltage stress and current stress on semiconductor devices, the number of components and conduction losses are being investigated.

The basic step-up dc-dc converters, boost whose the output gain voltage M=1/(1-D) , D is duty cycle, buck -boost, SEPIC, CUK and ZETA M=|D/(1-D)| cant not does provide a steep step up gain voltage [4]. In order to achieve high dc gain, the basic boost would be operating at a very high duty cycle large than 0.8, but this unrealistic cap for conduction time of recovery diode. Also, operation at high switching frequency cannot possible due to the diode does not turn on/off instantaneously [4, 5].

The alternative available solution to reach large dc gain, high switching frequency transformer or coupled inductor, but this would not be an exact solution due to losses of leakage inductances, cost and sizing, EMI problem, high voltage stress and reducing efficiency. Another solution, use a cascade of the boost converter (quadratic converters). In a cascade converter, the overall performance and efficiency depend on the product of each stag's which implies the attracting losses of energy [6].

The switching capacitor (SC) cell and switching inductor (SL) cell can provide a high dc gain ratio by charge the inductor or capacitor in parallel and discharge in series [4]. The SC cell composed of capacitor and diode only no inductor, therefore their size is small. The output voltage of SC converter depends on a number of capacitors only, for an ideal component, the output equal to V_out=(1+n) V_in [7]. However, the major issues of SC converters are low efficiency due to poor of a voltage regulator which implies does not able to use the full capacity of capacitor to transfer to load [4–7]. Also, increasing numbers of capacitor needed more switching device which means more losses. Regarding to SL cell can provide high dc a gain ratio. However, main issues of the SL cell are cost and sizing. Recently, the significantly advanced of DC-DC converters in order to achieve advanced topology with high efficiency and high power density, the Voltage Lift (VL) has been proposed [5–8]. These converters are combining from SC cell and SL cell. The key problem of VL converter is using more inductor and capacitor as inner storage elements.
In literature, many researchers have proposed a transformerless step up DC-DC converters in order to achieve large DC gain ratio. In [1], its combination the SL and SC to provide a high DC gain ratio. However, this converter cannot extendable and the voltage regulated is poor. The extendable boost converter has been proposed by [2]. The merits of this proposed is generated high dc gain at lower duty cycle lower than 0.4. However, the structure is very complex and at responsible duty cycle (0.5 – 0.65), the output dc gain is gradually decreased. In [3] and [19], The extendable non-isolated boost converters based on Active-Passive Inductor Cells (APICs) have been proposed. The features of these converters are provided very high dc gain voltage and can extendable by adding APICs. Nevertheless, the structure of these converters is very complex and very hard control due to exist of five or seven active switch and more number of active switches is increased in case of adding a new APICs. In [4], the switching inductor and capacitor is integrated

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into a basic boost converter. The structures and principles operation of these converters are very simple. However, the issue of these converters is voltage stress on active switch equal to output voltage. The modified boost converters have been proposed by [5]–[15] in order to obtain large dc gain and reduction voltage and current stresses on diodes and active switches. However, some of these converters have more switch which implies complex control drive. thereby, the extendable of these converters are very complex. In order to improve conventional boost converters and reduce current ripple as well as separate input current about output current to overcome input current pulsating, the couple inductor is used in [16]–[18], [22]–[24], and also [27].

In this paper, a new voltage lift cell can integrate into a family of the boost converters to achieve high dc gain voltage has been proposed. the proposed cell is designed by combining the merits of SC cell and SL cell. the significant benefits of a proposed cell are high output dc gain ratio, the low voltage stress on a switch, low current stress through switches which leads to low conduction losses and simple structure and control.

2. Proposed Converter

2.1. Analysis of Power Circuit Diagram of the Proposed Converter

In this paper, a new converter has been proposed as shown in Fig. 1(a). The proposed converter is composed of five inductors (L_1, L_2, L_3, L_4 and L_5), four capacitors (C_1, C_2 , C_3 and C_o), and eight diodes (D_1, D_2, D_3, , D_4, , D_5, , D_6, , D_7, and D_o). The first principle of converter is all inductors and capacitors are charged in parallel by Vin during turn on switch and discharge in series during turn off the switch.

Fig. 3 shows characteristics waveforms of a converter in steady state. The following assumptions are used to simplify the DC analysis: i) all elements are ideal, ii) the value of all capacitors are large in order to get constant output voltage, and iii) assume the proposed converter is operating under steady-state, which indicates the output is constant. The operating principles and the equations of voltage and current during CCM and DCM in steady state are discussed in details as follows.

Analysis of Proposed Converter in CCM

The equivalent circuit of a proposed converter during CCM is shown in Fig. 1(b) and 1(c) respectively. The analysis of CCM depends on two modes as follows:

Mode I: [0, DT] during this periodic, the switch S is turn on. The equivalent circuit of this mode is shown in Fig. 1(b). The reactive switching (L_1, C_1, L_2 and C_2) are charged in parallel by V_{in}. In addition, the diodes (D_1&D_2) are forward biased and D_o is reversed biased. The voltage across inductors and capacitors can be expressed as:

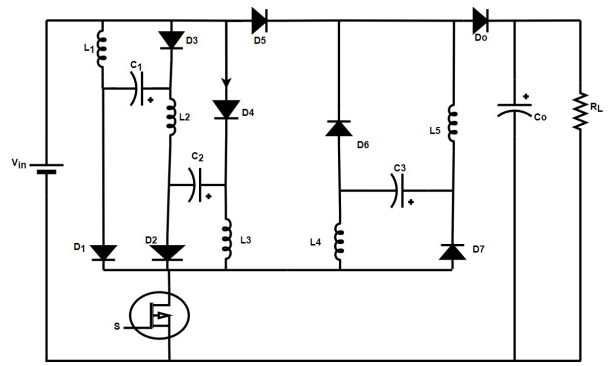
$$\begin{cases} V_L = V_{L1} = V_{L2} = V_{L3} = V_{L4} = V_{L5} \\ V_C = V_{C1} = V_{C2} = V_{C3} \\ V_{in} = V_c = V_L \end{cases} \quad (1)$$

During switch S-on period, the inductor current i_{L_1} is increased linearly and voltage cross inductor is equal V_{in} ,and also, the current inductor is decreased linearly during switch off period. With applying volt-second balance, the voltage across L_1 during off period is,

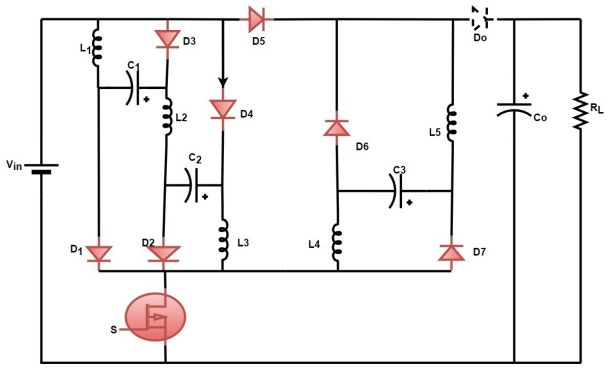
$$[V_{L_{1-off}} = -\frac{D}{1-D} V_{in} \quad (2)$$

Mode II: [DT, T] during this periodic, the switch S is off, the reactive switching (L_1, C_1, L_2, C_2) are discharged in series respectively. Moreover, the diodes (D_1, D_2 &D_3) are reversed biased, and D_o is forward biased as shown in Fig. 1(c). By applied KVL, the voltage across inductor L_2 is,

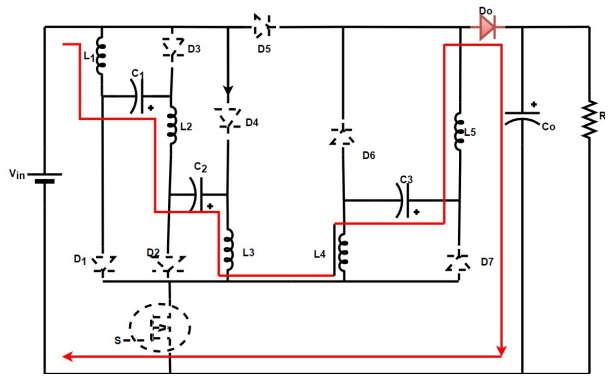
$$V_L = \frac{4V_{in} - V_O}{5} \quad (3)$$



(a)



(b)



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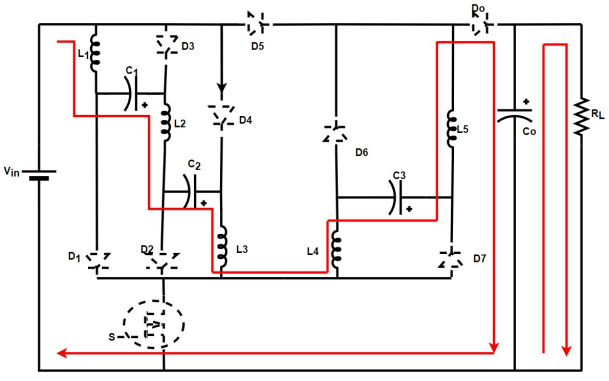


(d)

Fig. 1: Proposed converter, (a) proposed circuit (b) path of charge during switch S-on (c) path of discharge during switch S-off (d) equivalent circuit during DCM.

With the volt-second balance principle for inductor L_2,

$$\int_0^{DT_S} V_{in}dt + \int_{DT_S}^{T_S} \frac{4V_{in} - V_O}{5} = 0 \tag{4}$$

By combining the equations (2) & (4), the output voltage of proposed converter is,

$$V_o = \frac{4+D}{1-D} V_{in} \tag{5}$$

The DC voltage gain ratio of a proposed conversion in CCM, G_{CCM} is,

$$G_{CCM} = \frac{V_o}{V_{in}} = \frac{4+D}{1-D} \tag{6}$$

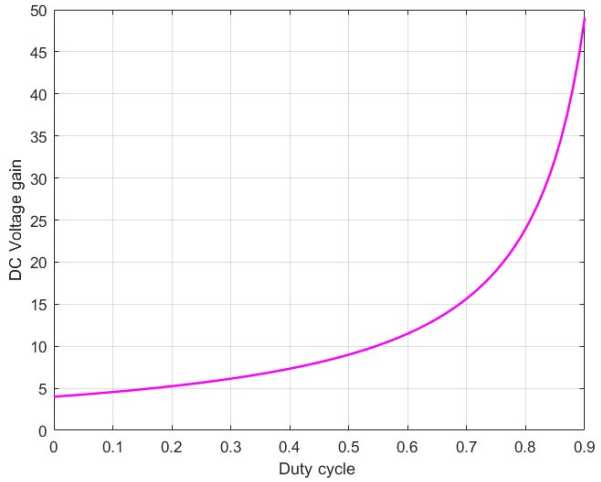


Fig. 2: Voltage transfer gain vs D

The curve of dc gain voltage against conduction duty cycle is shown in Fig. 2 Since considering all passive element and semiconductors device are ideal, therefore $p_o = p_{in}$ and the input current is,

$$I_{in} = \frac{4+D}{1-D} I_o = \frac{4+D}{1-D} \frac{V_o}{R} \tag{7}$$

During switch on period, the charge of output capacitor C_o is decreased and increased during the switch-off period. Therefore, the charge across C_o during each switching cycle in steady state is,

$$Q_{C_{O+}} = I_o DT \& Q_{C_{o-}} = I_{C_{o-off}}(1-D)T \tag{8}$$

With each switching cycle $Q_{C_{O+}} = Q_{C_{O-}}$, therefore, the current of a capacitor during off period is,

$$I_{C_{O-off}} = \frac{D}{1-D} I_o \tag{9}$$

The current of a diode D_o during switching off period is,

$$I_{D_{o-off}} = I_{C_{o-off}} + I_o = \frac{1}{1-D} I_o \tag{10}$$

Also, the current of inductors and capacitors during off period are,

$$I_L \ = I_{C_{-off}} = I_{D_{o-off}} = \frac{1}{1-D} I_o \tag{11}$$

The charge of capacitor C_1 is increased during on period and decreased during off period, therefore, in each switching cycle $Q_{C_{1+}} = Q_{C_{1-}}$ and thereby, the current of capacitor during on period is,

$$I_{C_{1-on}} = \frac{1-D}{D} I_{C_{1-off}} = \frac{1}{D} I_o \tag{12}$$

Analogously, the current of a capacitor C_2 during on period is,

$$I_{C_{2-on}} = \frac{1-D}{D} I_{C_{2-off}} = \frac{1}{D} I_o = I_{C_{-on}} \tag{13}$$

Since the peak-to-peak current of inductors (i_{L1}&i_{L2}) during on period $\Delta i_{L_1} = \frac{V_{in}DT}{L_1}$ and $\Delta i_{L_2} = \frac{V_{in}DT}{L_2}$. Therefore, the variation ratio of (i_{L1}&i_{L2}) are,

$$\xi_{L_1} = \frac{\frac{\Delta i_{L1}}{2}}{I_{L_1}} = \frac{(1-D)\,D}{2G_{CCM}} . \frac{R}{fL_1} \tag{14}$$

$$\xi_{L_2} = \frac{\frac{\Delta i_{L2}}{2}}{I_{L_2}} = \frac{(1-D)\,D}{2G_{CCM}} . \frac{R}{fL_2} \tag{15}$$

And similarly for all inductors.

The current variation of diode i_{D_o} in off stage is equal to Δi_{L_5} and the current variation equal to $\frac{V_{in}DT}{L_5}$. Therefore, the variation ratio of i_{D_o} is,

$$\xi_{D_o} = \frac{\frac{\Delta i_{L5}}{2}}{I_{D_{O-off}}} = \frac{(1-D)\,D}{2G_{CCM}} . \frac{R}{fL_5} \tag{16}$$

The peak-to-peak voltage of the output capacitor Δv_o is equal to $\frac{\Delta Q}{C_o}$ and $\Delta Q = DTI_o$. Therefore, the variation of voltage v_o is,

$$\varepsilon_{v_o} = \frac{\frac{\Delta v_o}{2}}{v_o} = \frac{D}{2fR\,C_o} \tag{17}$$

Analysis of Proposed Converter in DCM

During switch off period, when the inductor fully discharged and the current of the diode will decrease to zero due to change in load and switching frequency, the converter will operate at DCM as shown in Fig. 3(b). In this case, only the output capacitor Co discharge to the load as shown in Fig. 1(b). Therefore, the condition for DCM is $\xi_{D_o} \geq 1$. Therefore,

$$\frac{(1-D)\,D}{2G_{CCM}} . Z_n \geq 1 \tag{18}$$

Where Z_n is normalized load $\frac{R}{fL_5}$

The graph of the boundary curve against the normalized load $\frac{R}{fL_5}$ is shown in Fig. 4. The converter will operate at the boundary of CCM and DCM if the current of the diode i_{D_o} decrease to zero at t=T as shown in Fig. 3(b), Therefore, the boundary between CCM and DCM can be written as

$$Z_{n-boundary} = \frac{2G_{CCM}}{(1-D)\,D} \tag{19}$$

The converter will operate at DCM if $Z_n > Z_{n-boundary}$. under condition of the DCM, i_{D_o}decrease to zero at t=t_1=$[D + m(1-D)]$T where:

$$DT < t_1 < T \ and \ 0 < m < 1 \tag{20}$$

Where m is the current filling efficiency [10] for lift converter circuit and defined as

$$m = \frac{t_1 - DT}{(1-D)\,T} \tag{21}$$

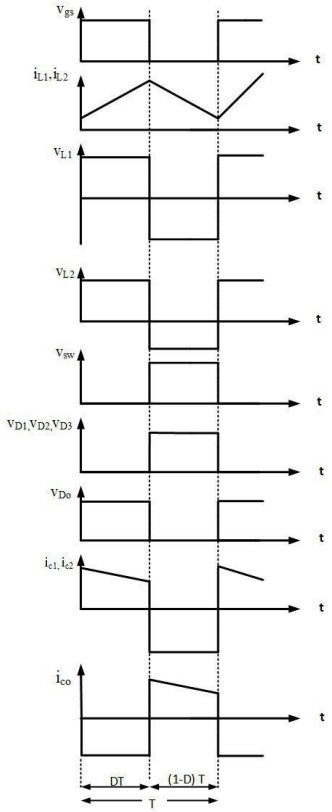
In DCM of operation, During switch S-on period, the inductor current i_{L_1} is increased linearly and voltage cross inductor is equal V_{in} and also, the current of inductor is decreased linearly during switch off period from DT to (1-D) mT. With applying volt-second balance, the voltage across L_1 during off period is,

$$V_{L-off} = -\frac{D}{(1-D)\,m} V_{in} \tag{22}$$

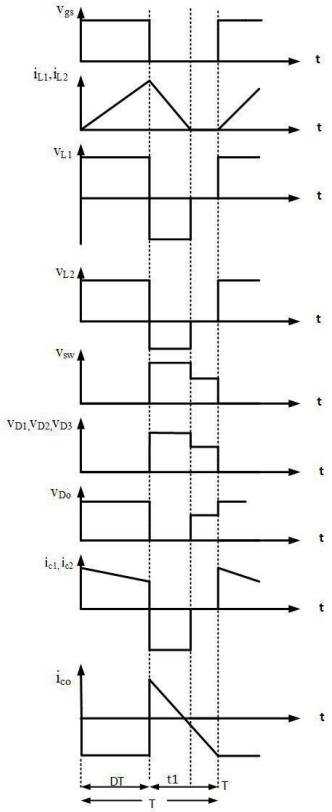
Similarly, in CCM the inductor current i_{L_2} increased linearly during on period and charge by Vin and also decreased linearly during off period from DT to (1-D) mT and the corresponding voltage across L_2 is

$$V_L = V_{in} - 5V_{L\ _{-off}} + V_{C_1} + V_{C_2} + V_{C_3} - V_o \tag{23}$$

Thus, by applying volt-second balance, we get



(a)



(b)

Fig. 3: Characteristics waveform (a) CCM (b) DCM

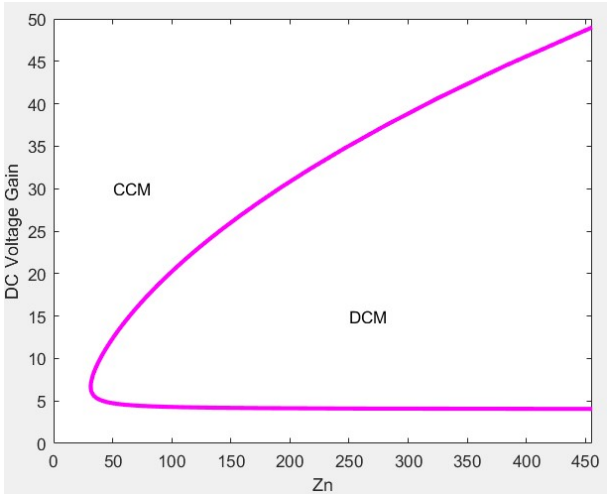


Fig. 4: The boundary between CCM and DCM

$$V_{in}DT + \left(V_{in} - 5V_{L_{1-off}} + V_{C_1} + V_{C_2} + V_{C_3} - V_o\right) (1-D)\,mT = 0 \quad (24)$$

During switching off period the transferred charges of inductor L_5 is equal to

$$\frac{V_o}{R}T = mT\ (1-D)\,\frac{DT\ V_{in}}{2L_5} \quad (25)$$

Finally, substituting (25) into (24) in order to obtain the conversion ratio of the proposed circuit in DCM as follows:

$$G_{DCM} = \frac{V_o}{V_{in}} = 2 + \sqrt{4 + 5D^2 Z_n/2} \quad (26)$$

Voltage Stress on Switching Devices

$$\begin{cases} V_{D_1} = V_o - 5V_{in} \\ V_{D_2} = V_o - 7V_{in} \\ V_{D_3} = V_o - 7V_{in} \\ V_{D_4} = V_o - 5V_{in} \\ V_{D_5} = V_o - V_{in} \\ V_{D_6} = V_o - 7V_{in} \\ V_{D_7} = V_o - 7V_{in} \\ V_{D_o} = V_o - V_{in} \\ V_s\ = V_o - V_{in} \end{cases} \quad (27)$$

Capacitors and Inductance Design

In order to more reduction of the voltage stress on switches and diodes, both inductor values are chosen with equal values. The inductor values can be calculated by considering the switching frequency (f_s) and inductor ripple current (ΔI_L) as,

$$L_1 = L_2 = L_3 = L_4 = L_5 = \frac{DV_{in}}{\Delta I_L f_s} \quad (28)$$

analogously, the design of the capacitor depends on switching frequency (f_s) and ripple voltage in capacitors (ΔV_C). The output capacitor can be designed from equation (17) as,

$$C_o = \frac{D}{2fR\ \varepsilon_{v_o}} \quad (29)$$

The values of switching capacitors can be calculated as,

$$C_1 = C_2 = C_3 = \frac{\Delta Q}{\Delta V_{C1}} = \frac{I_{in}(1-D)}{2f_s \Delta V_{C1}} \quad (30)$$

By substitute equation (7) in equation (32) and considering the converter is lossless, the values of capacitors can find out as,

$$C_1 = C_2 = C_3 = \frac{(4+D)\,V_o}{2Rf_s\Delta V_{C1}} \tag{31}$$

Where $\Delta V_{C1} = \Delta V_{C2} = \Delta V_{C3}$.

3. SIMULATION AND EXPERIMENTATION RESULTS

In this section, in order to confirm the theoretical analysis of the proposed transformerless step-up converter, the simulation software Matlab/Simulink is applied to the proposed circuit. Also, the prototype circuit was built in the laboratory of power electronics. The proposed converter is implemented in CCM mode as follow:

3.1. CCM

The specification of proposed circuit and components in simulation and hardware are selected as, V_{in}=24V, R=668Ω, $L_1 = L_2 = L_3 = L_4 = L_5 = 0.667mH$, $C_1 = C_2 = C_3 = C_o = 100\mu F$, $f_s = 20kHz$, and D=0.5. Moreover, MOSFET IRFP460N (40A,600V) is selected for S_1, and ultrafast diode (MUR4060pt) (40A,600V) for all diodes. To calculate the boundary of normalized load and normalized load, we use equations (18) and (19), the $Z_{n-boundary}|_{D=0.5} = 72$ and Z_n=49.851 , which means the above parameters are appropriated for CCM mode operation. To evaluate the theoretical output voltage V_o and inductors currents $I_{L_1} = I_{L_2}$, we use equations (5) and (11). The output voltage V_o=216V, I_o=0.323A and IL=0.64671A, respectively. The TLP350 is used as drive circuit for active switch. The control voltage based Pulse width modulation (PWM) is used for drive the proposed converter.

The simulation results of output voltage and output current are demonstrated in figures 7 & 8. It can be seen from these figures, the simulation results are matching to the theoretical results and also the experimental output voltage is also matching with the theoretical and simulation results Vo=216V as depicted in Fig. 9 at conduction duty cycle (D=0.5) as shown in Fig. 6. The efficiency of proposed converter up to 97.4%. According to the (1), the voltage across each inductor equal to Vin which investigating in the experimental results as shown in figures 10 & 11. The voltage across the three boost capacitors are illustrated in figures 12 & 13. It can be observed from these figures; the output waveforms are same the theoretical calculation according to the (1) V_{in}=V_C=24V.

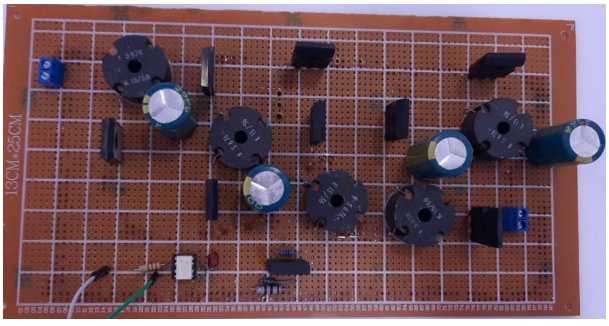


Fig. 5: prototype circuit of proposed converter.

The voltage stress across the output diode and diode (5) that indicated the proposed circuit (see figure (1)) is equal according to the equations (28). Figures 14 & 15 indicated the output voltage across the diodes and investigating the equations.

Finally, the voltage stress of active switch is illustrating in Fig. 16. The simulation results prove that the proposed converter is robustness and it has high efficiency.

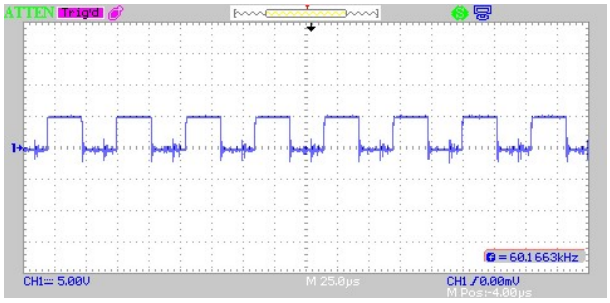


Fig. 6: Duty cycle D=0.5.

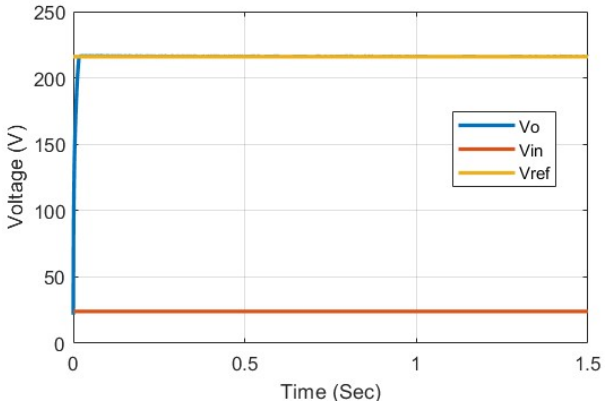


Fig. 7: Simulation output voltage of proposed converter

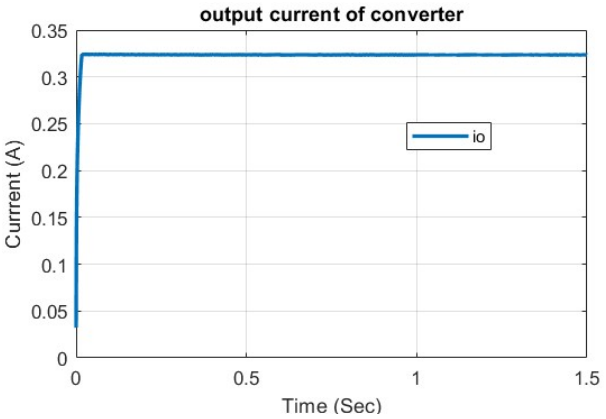


Fig. 8: Simulation output current of proposed converter

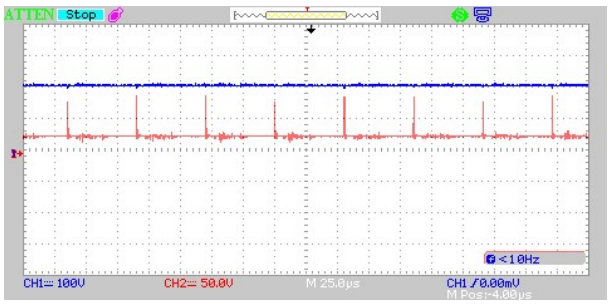


Fig. 9: Experimental output voltage of proposed

4. CONCLUSION

In this paper, a novel non-isolated high-up DC-DC converter is suggested. The suggested converter's design and operation are straightforward. With a low duty cycle, it can produce a significant

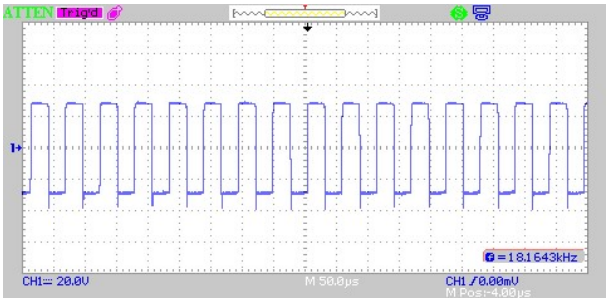


Fig. 10: Inductor voltages V_{L1},V_{L2},V_{L3}

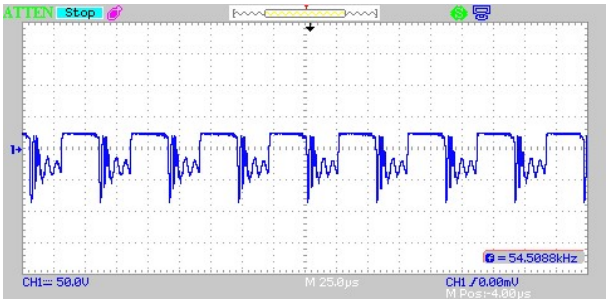


Fig. 11: Inductor voltages V_{L4}, VL_5

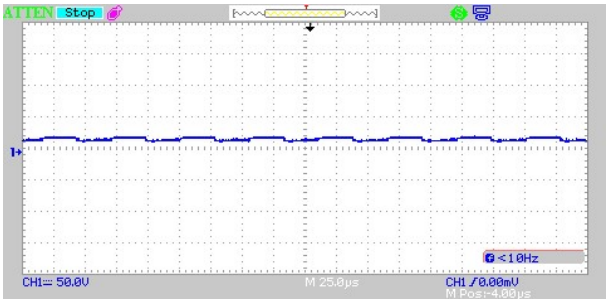


Fig. 12: Capacitor voltage V_{C1}

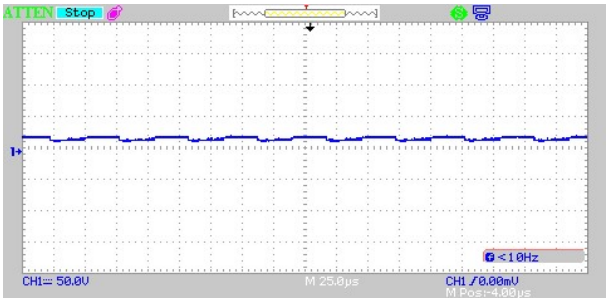


Fig. 13: Capacitor voltage V_{C2}

DC gain. According to theoretical studies, the proposed circuit has a low voltage stress on the active switch and can be selected to employ active switches with low voltage ratings and low impedance levels. The steady-state analysis of voltage gains as well as the border operating state are thoroughly investigated. Finally, a laboratory prototype circuit of the suggested circuit was built to demonstrate the theoretical analysis. The outcomes of the experiments demonstrate that a higher step increase is possible. The suggested converter has a 97.4% efficiency.

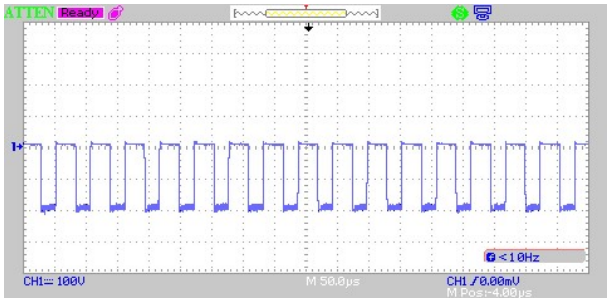


Fig. 14: Output diode voltage V_{d5}

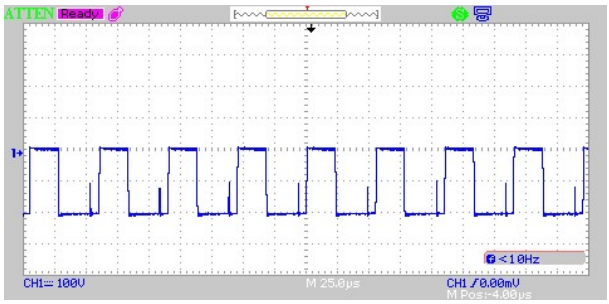


Fig. 15: Output diode voltage V_{do}

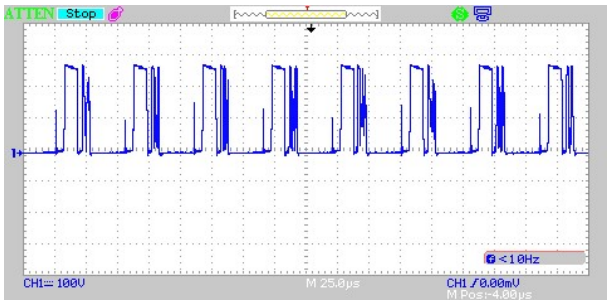


Fig. 16: Output switch voltage V_S

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